

BMW Z4 14" Schematics Document

Ivy/Sandy Bridge Panther Point

2012-04-02
REV : A00

DY : None Installed
UMA: UMA only installed
SG: PX solution installed.

<Core Design>



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Title

Cover Page

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A3

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BMW Z4 DIS

Rev

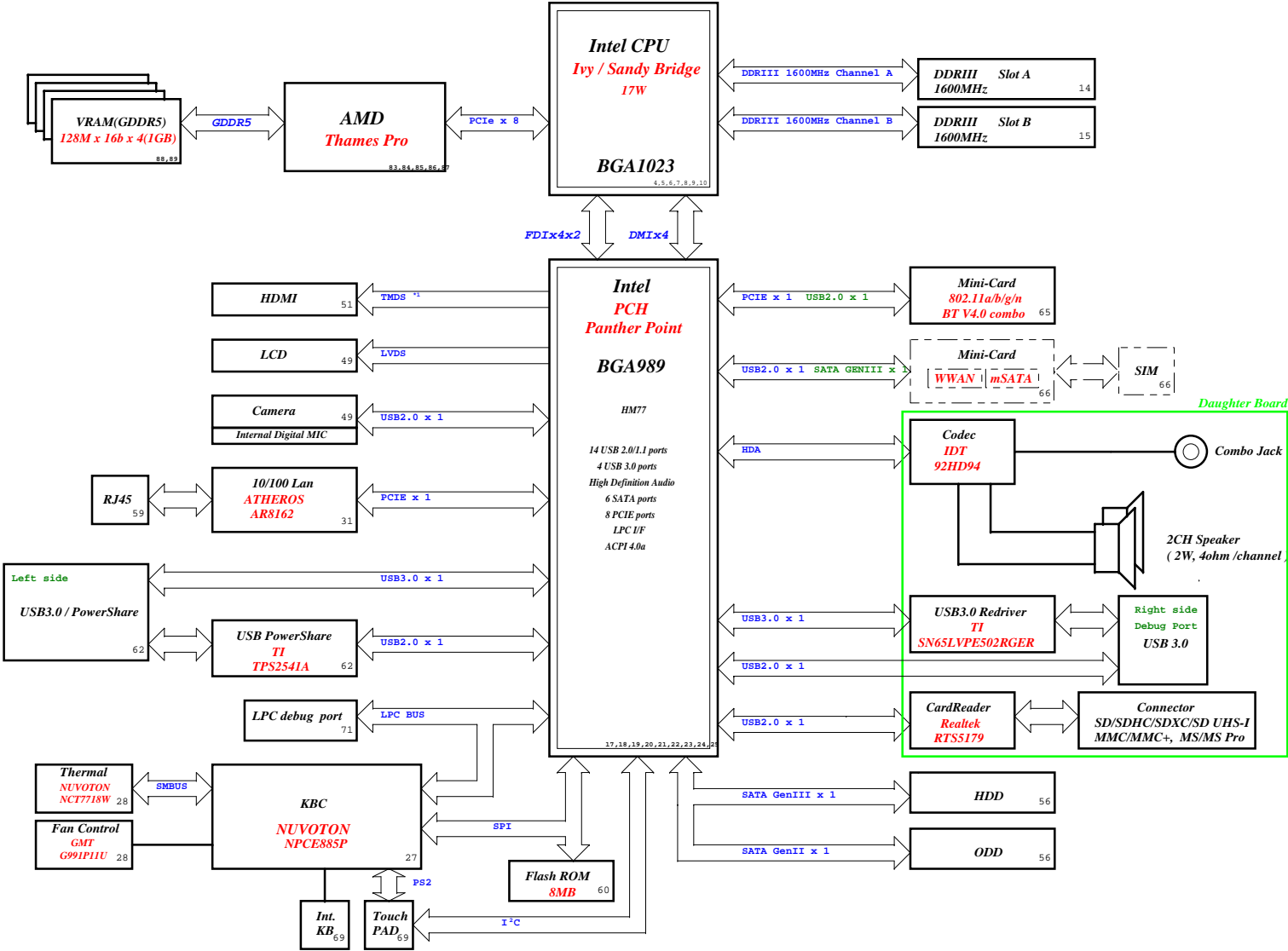
A00

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Block Diagram
(Discrete / UMA)

Project Code: 91.4UV01.001
PCB P/N : 48.4SB02.011
Revision : 11289-1



CHARGER		40
BQ24727		
INPUTS	OUTPUTS	
AD+	BT+	
SYSTEM DC/DC		41
TPS51125RGER		
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5	
CPU DC/DC		42,43
VT1318+VT1326		
INPUTS	OUTPUTS	
5V_S5	VCC_CORE	
GFX DC/DC		44
VT1318+VT1323		
INPUTS	OUTPUTS	
5V_S5	VCC_GFXCORE	
SYSTEM DC/DC		45
VT386		
INPUTS	OUTPUTS	
5V_S5	1D05V_PCH VCCP_CPU	
SYSTEM DC/DC		46
VT385(DIS)/RT9026 VT386(UMA)/RT9026		
INPUTS	OUTPUTS	
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	
SYSTEM DC/DC		47
RT8068A		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S0	
SYSTEM DC/DC		48
APL5916		
INPUTS	OUTPUTS	
VCCP_CPU	0D85_S0	
VGA DC/DC		92
VT358		
INPUTS	OUTPUTS	
5V_S5	VGA_CORE	
VGA DC/DC		93
APL5930		
INPUTS	OUTPUTS	
1D5V_S3	1V_VGA_S0	
Switches		
INPUTS	OUTPUTS	
1D5V_S3 5V_S5 3D3V_S5 3D3V_S5 1D8V_S0 1D5V_S3	1D5V_S0 5V_S0 3D3V_S0 3D3V_MLAN_ACAC 3D3V_VGA_S0 1D8V_VGA_S0 1D5V_VGA_S0	
UMA/Discrete		
PCB LAYER		
L1:Top	L5:VCC	
L2:GND	L6:Signal	
L3:Signal	L7:GND	
L4:Signal	L8:Bottom	

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Block Diagram

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*1: Transition minimized differential signaling

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
INTVRMEN	Integrated 1 V VRMs is enabled when high, External when low.
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
DF_TVS	DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor.
HAD_DOCK_EN# /GPIO[33]	This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0) Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

Power Plane

Power Plane	Voltage	Actice Status	Description
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1V_S0 0D85V_S0 0D75V_S0 VCC_CORE VCC GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1V 0.85V 0.75V 0.3V to 1.3V 0 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

Sandy & Ivy Bridge Compatibility

Pin Name	Configuration	Schematic Notes
DDR3 VREF	Sandy Bridge + Ivy Bridge	DDR3 VREF, M1 and M3 function are required.
	Ivy Bridge	No change.
PROC_SELECT# & DF_TVS	Sandy Bridge + Ivy Bridge	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH VccDFTERM rail.
	Ivy Bridge	No change.
VCCIO_SEL	Sandy Bridge + Ivy Bridge	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a need for a separate VR for the processor at 1.0 V and the PCH at 1.05 V. A single VR may be shared for both.
	Ivy Bridge	No change.
VCCSA_VID[0:1]	Sandy Bridge + Ivy Bridge	VCCSA[0:1] are the select pin of VCCSA's power control.
	Ivy Bridge	No change.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value	POP Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1	0
CFG[4]		1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	1	1
CFG[6:5]	PCI-Express Port Bifurcation Straps	11: 1x16 PCI Express 10: 2 x8 - PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express	11	10

USB Table

Pair	Device
0	USB3.0 port1, with Power Share
1	USB3.0 port2, debug port
2	NC
3	NC
4	Touch Panel
5	NC
6	NC
7	NC
8	WWAN
9	NC
10	Card reader
11	WLAN
12	CAMERA
13	NC

PCIE Table

PCIE	
Lane	Device
1	NC
2	NC
3	NC
4	WLAN
5	NC
6	Onboard LAN
7	NC
8	NC

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	NC
3	NC
4	ODD
5	NC

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SSID = CPU

WWW.AliSaler.Com

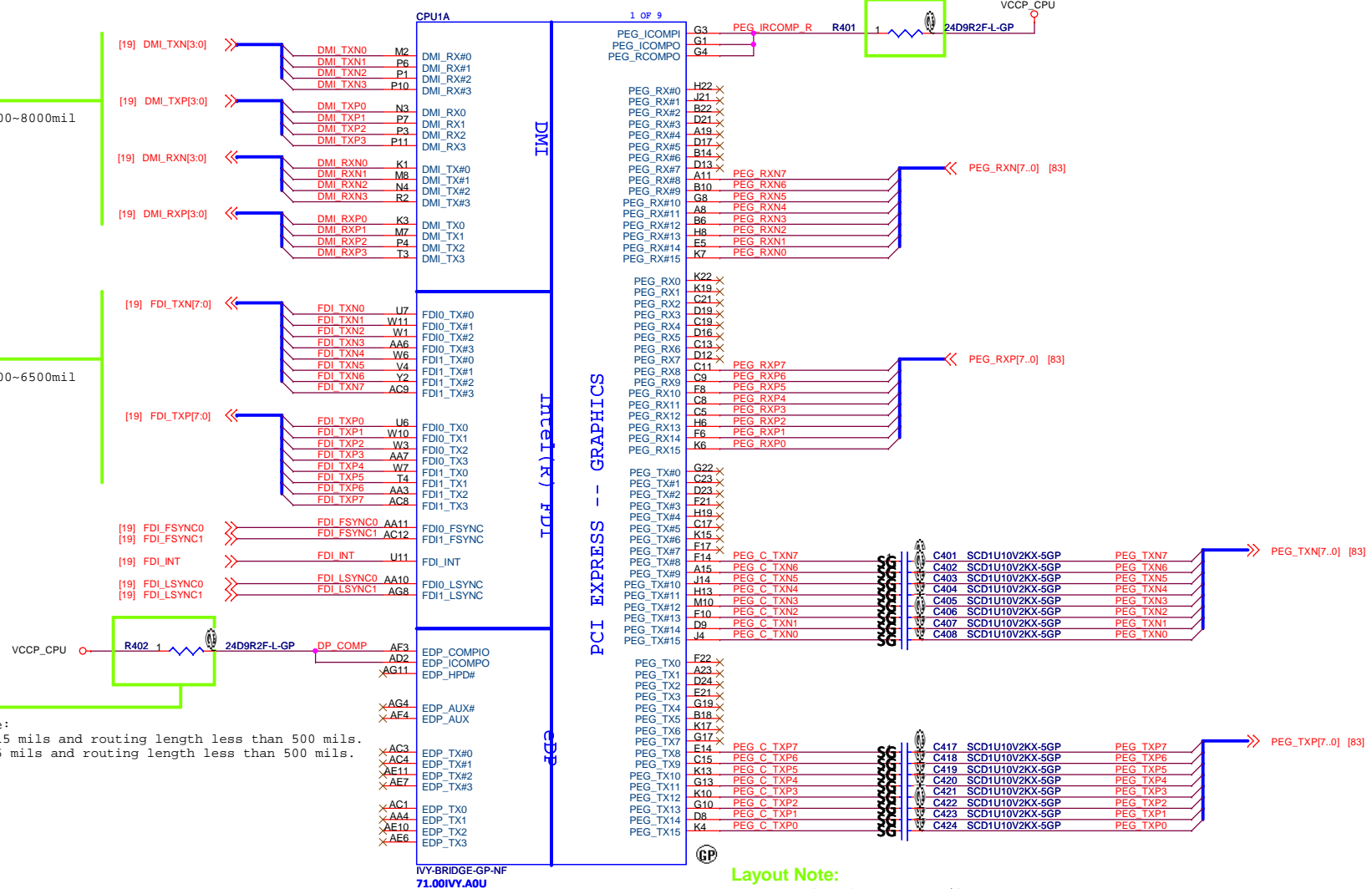
Layout Note:
DMI trace length 2000~8000mil

Layout Note:
FDI trace length 2000~6500mil

Layout Note:
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:
PEG trace length 1500~9000mil

Layout Note:
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



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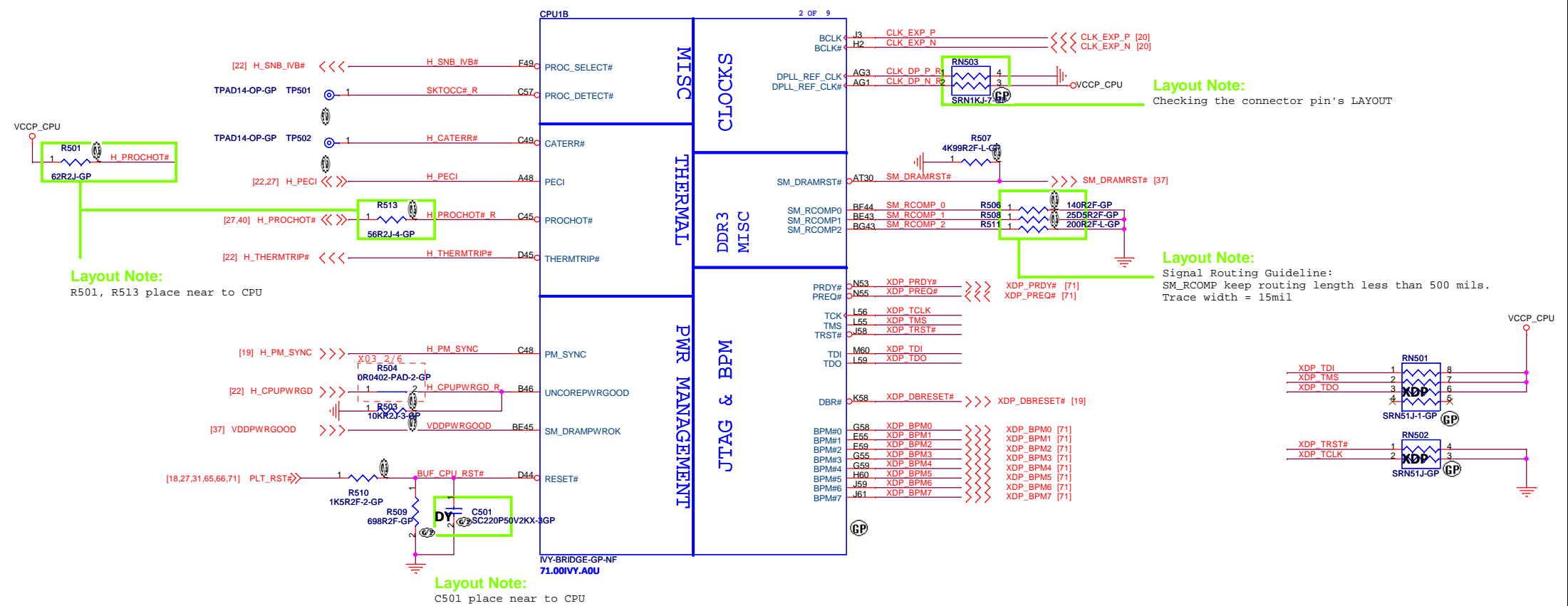
Title: **CPU(PCIE/DMI/FDI)**

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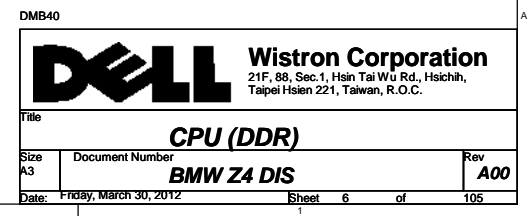
WWW.AliSaler.Com

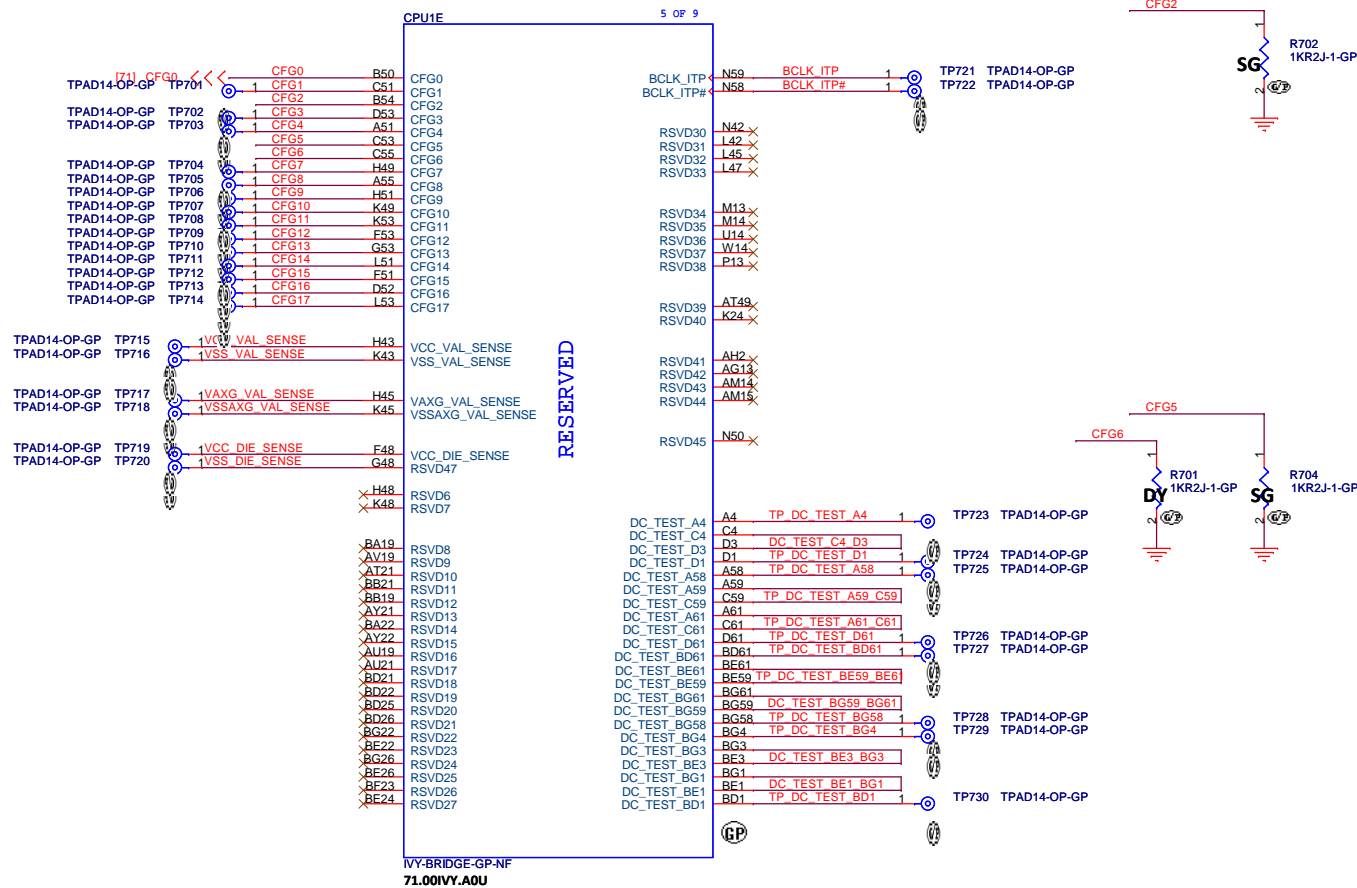
SSID = CPU



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PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

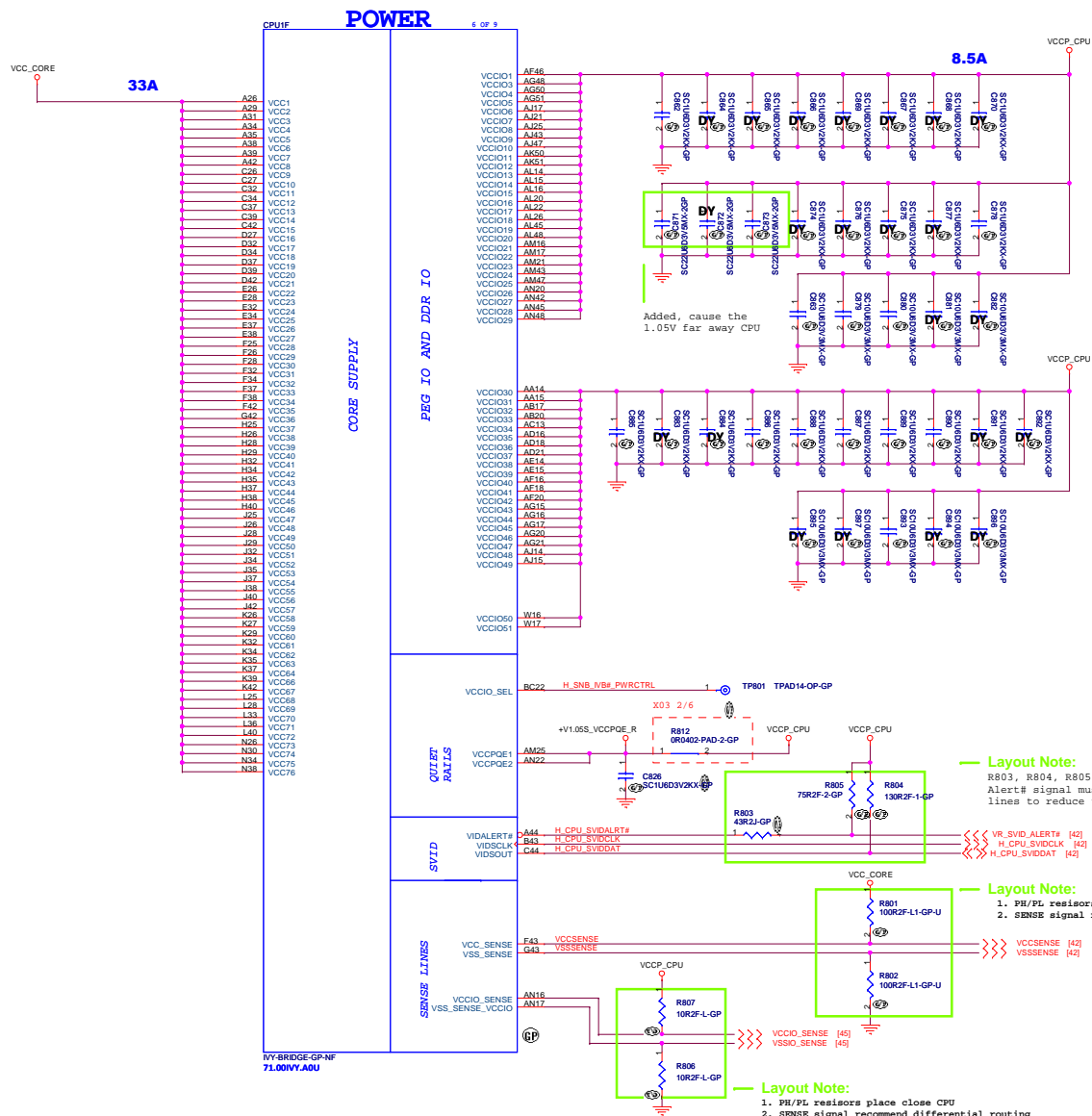
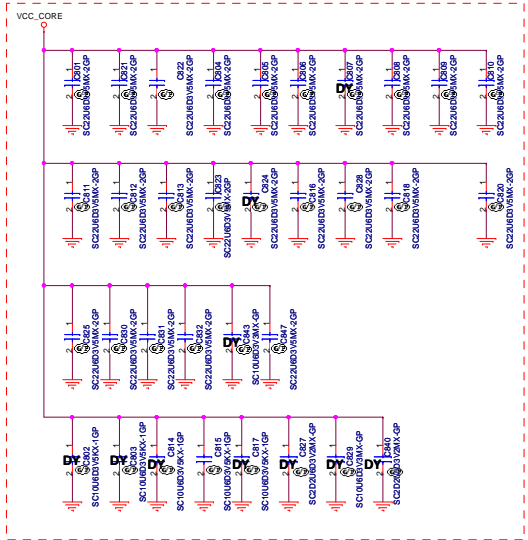
Display Port Presence Strap	
CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: 1x16 PCI Express 10: 2 x8 - PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express

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X01 12/21
X01 12/16
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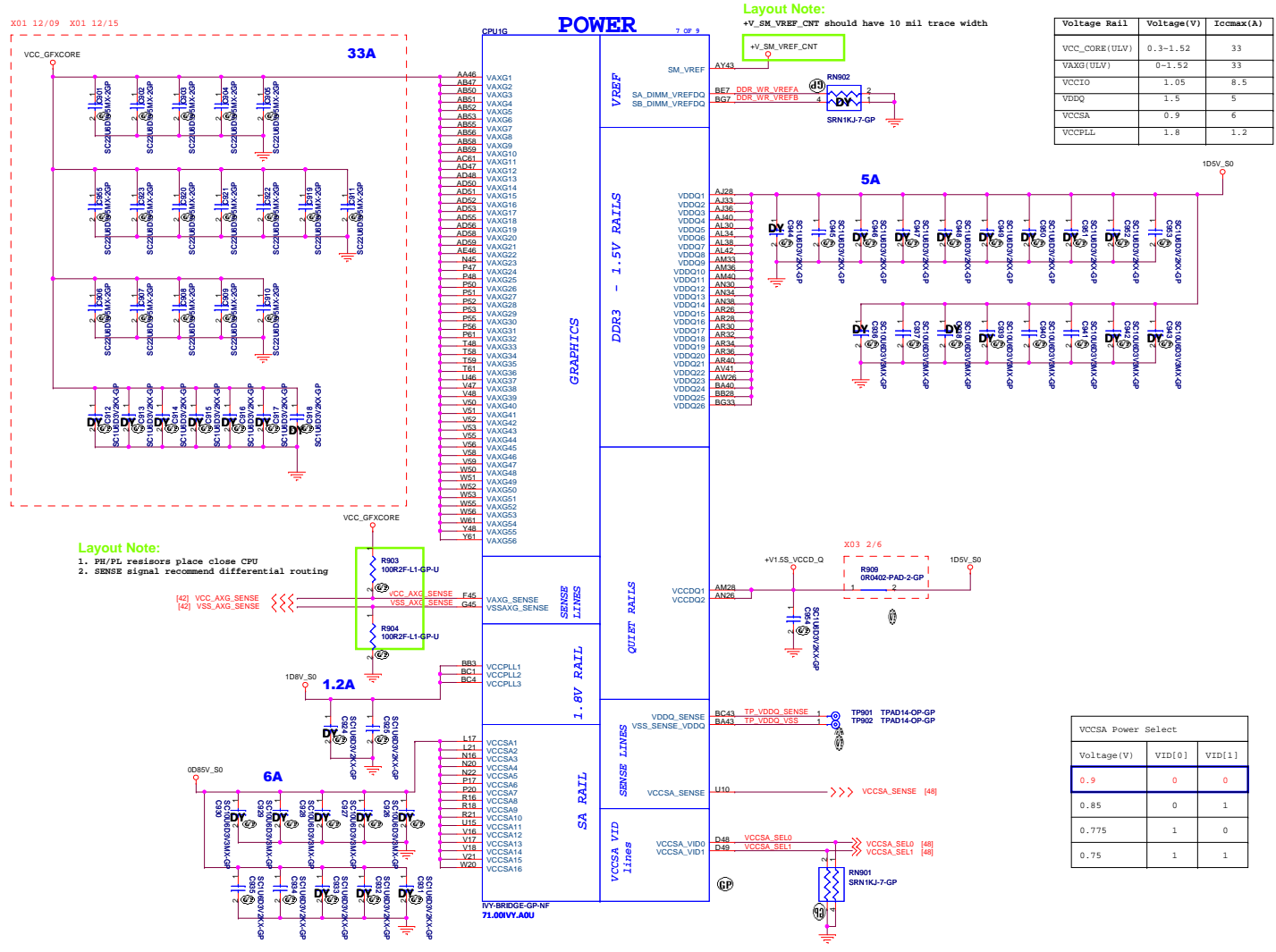


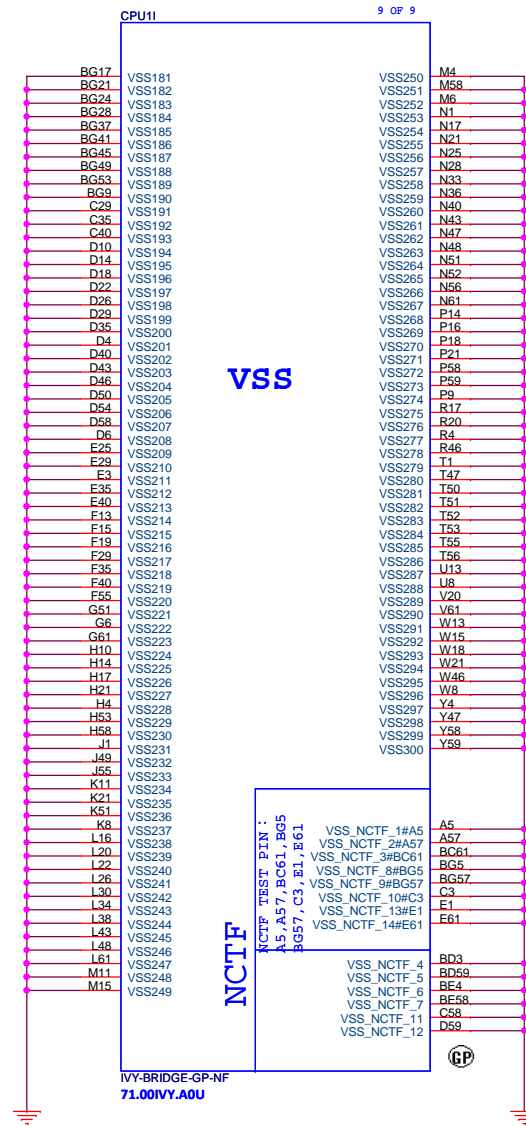
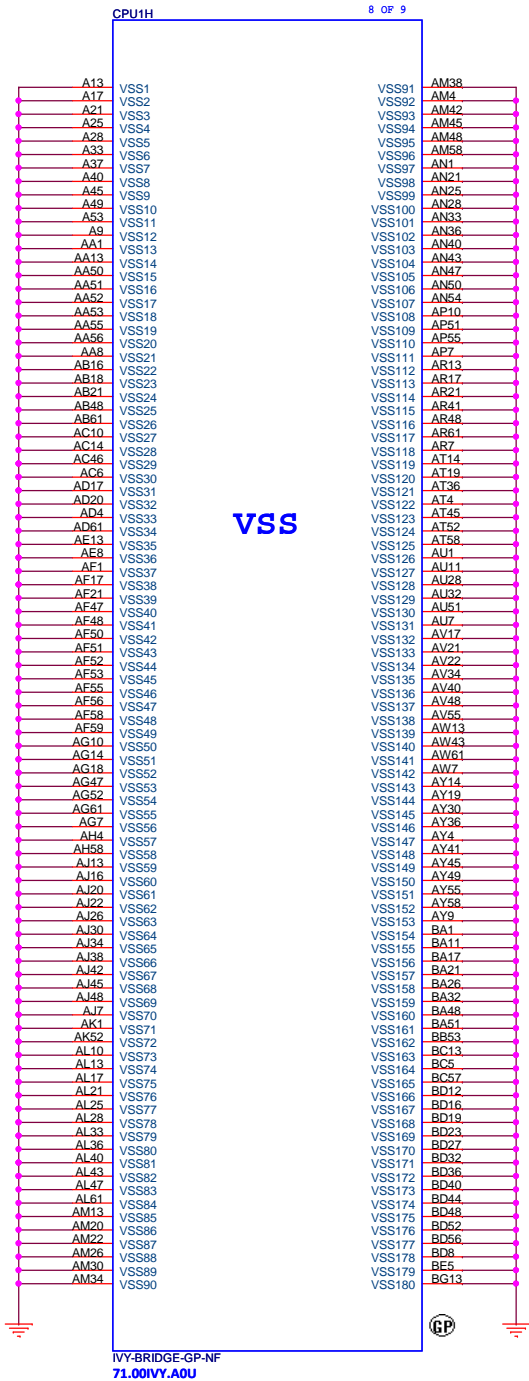
Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE (ULV)	0.3-1.52	33
VAXG (ULV)	0-1.52	33
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.9	4
VCCPLL	1.8	1.2

Layout Note:
R803, R804, R805 need close to CPU
Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them

Layout Note:
1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

Layout Note:
1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing





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CPU (VSS)

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XDP

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Title

(Reserved)

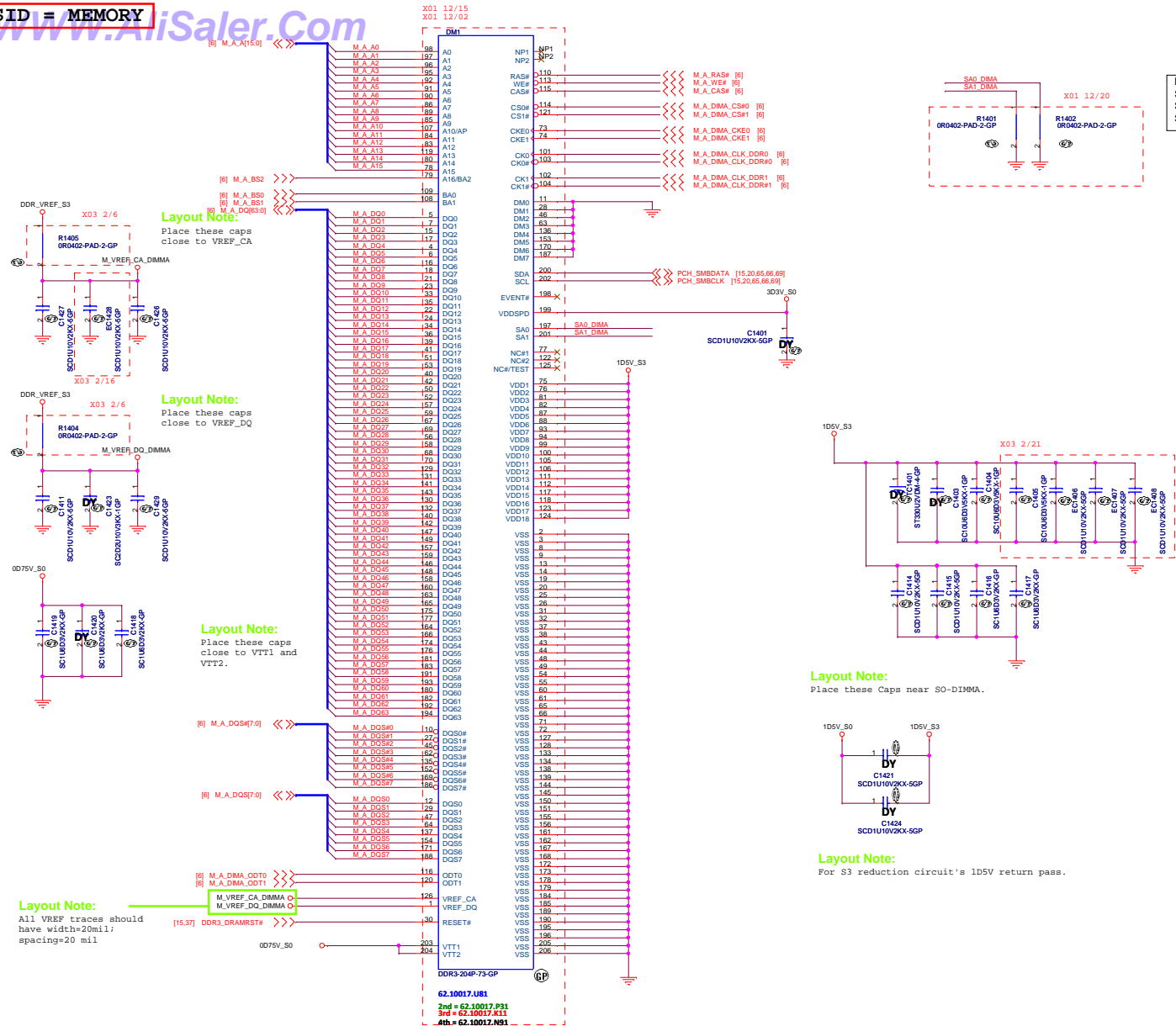
Size
A3

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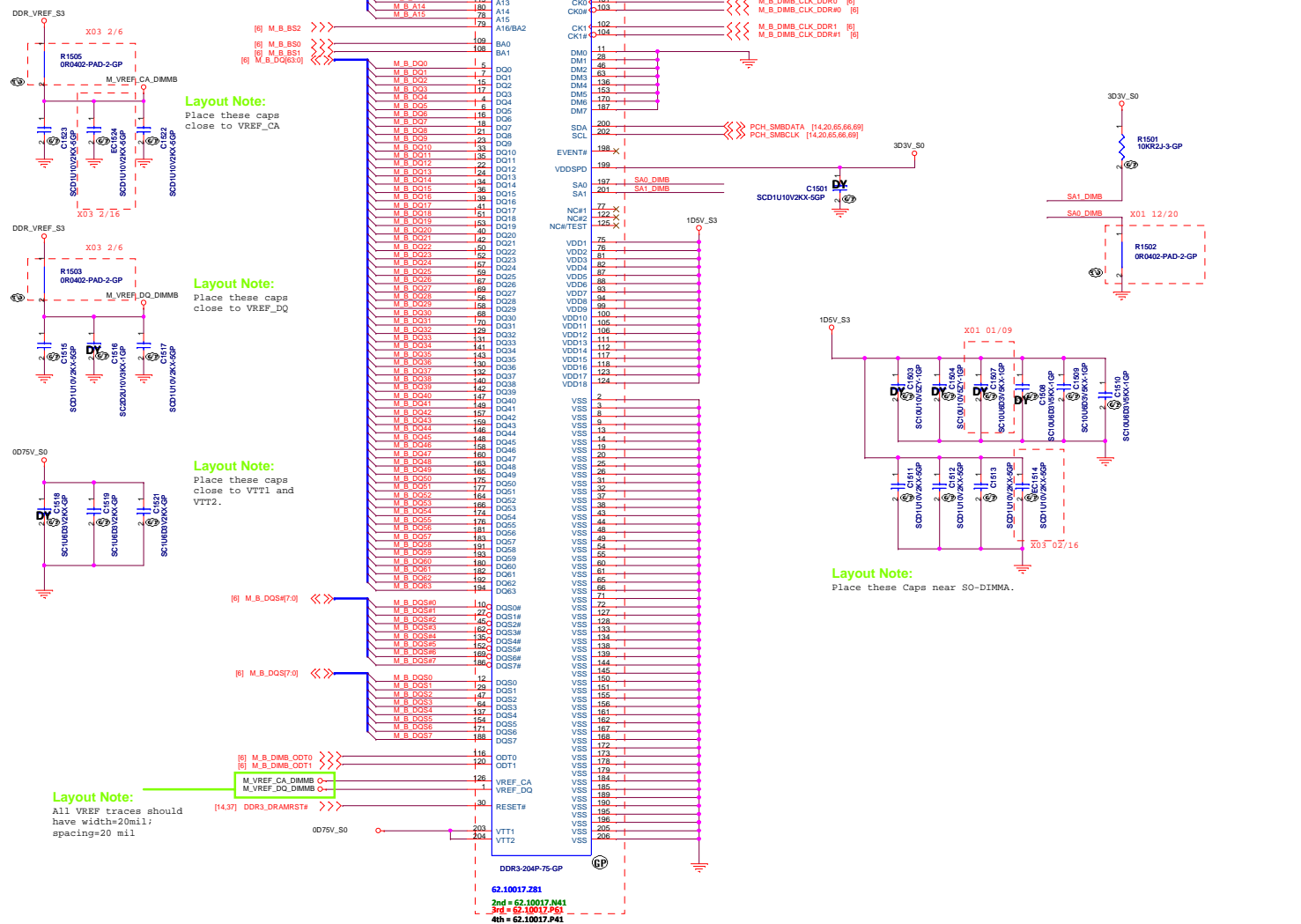
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Note:
SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
For S3 reduction circuit's 1D5V return pass.



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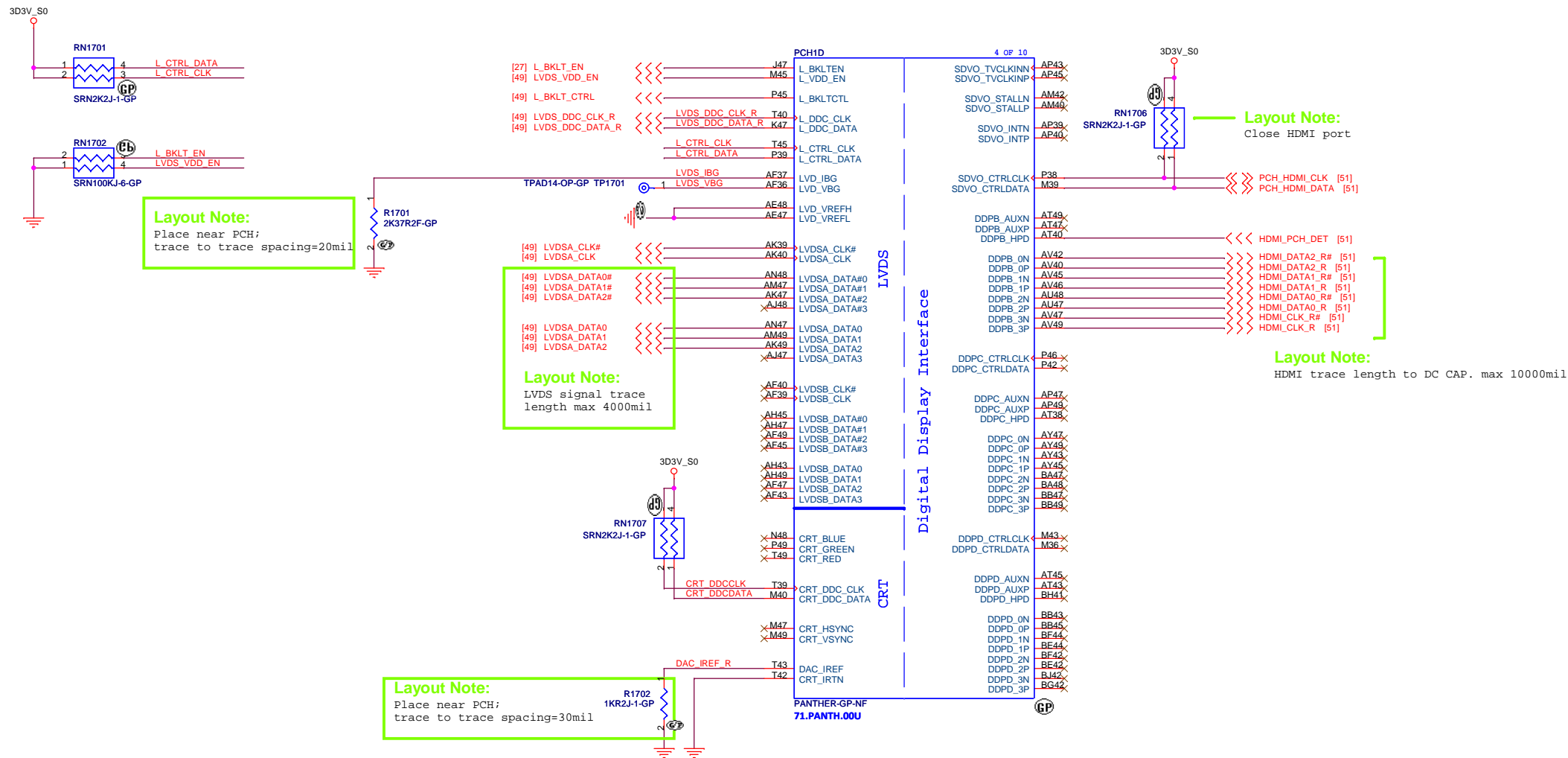
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Reserved

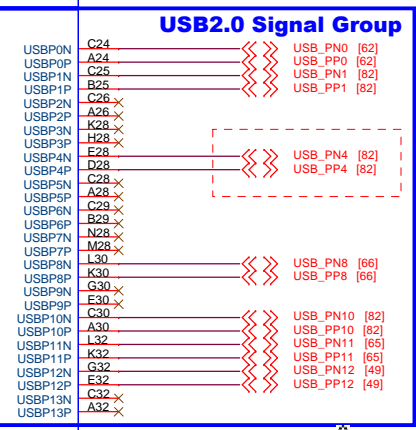
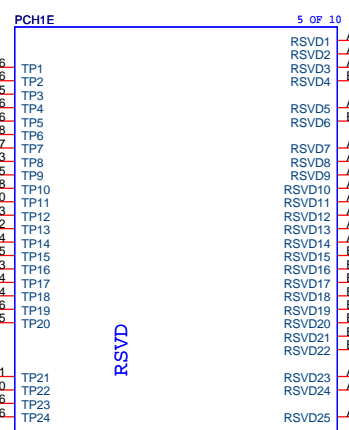
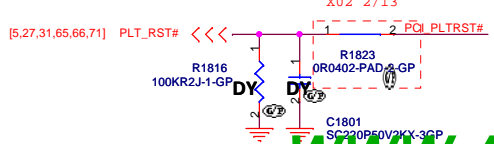
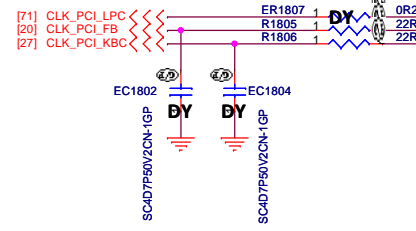
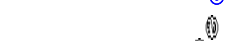
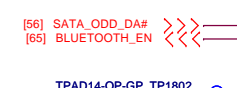
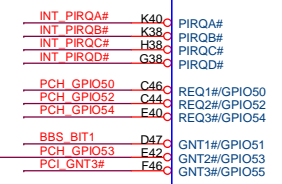
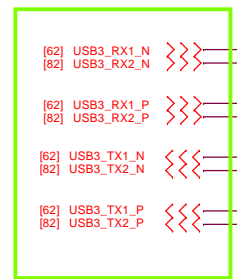


SSID = PCH

USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

Layout Note:
Trace Length :
PCH ~9000mil~~Cap~~1000mil~~CONN



USB Table

Pair	Device
0	USB3.0 port1, with Power Share
1	USB3.0 port2
2	NC
3	NC
4	Touch Panel
5	NC
6	NC
7	NC
8	WWAN
9	NC
10	Card reader
11	WLAN
12	CAMERA
13	NC

1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.

Layout Note:

1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



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PCH (PCI/USB/NVRAM)

BMW Z4 DIS

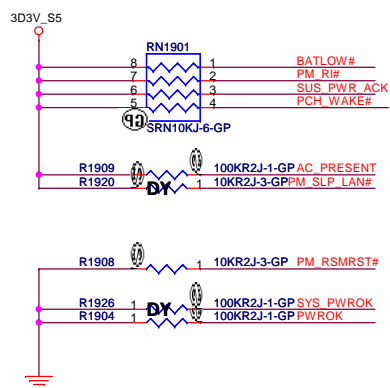
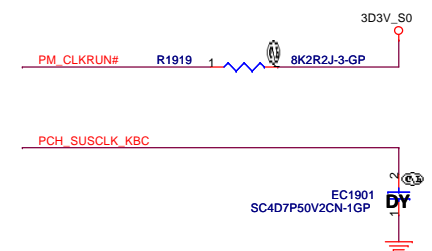
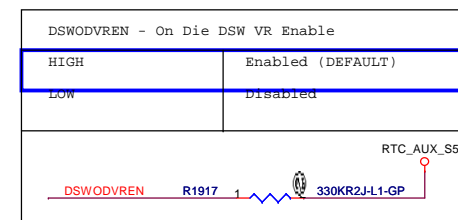
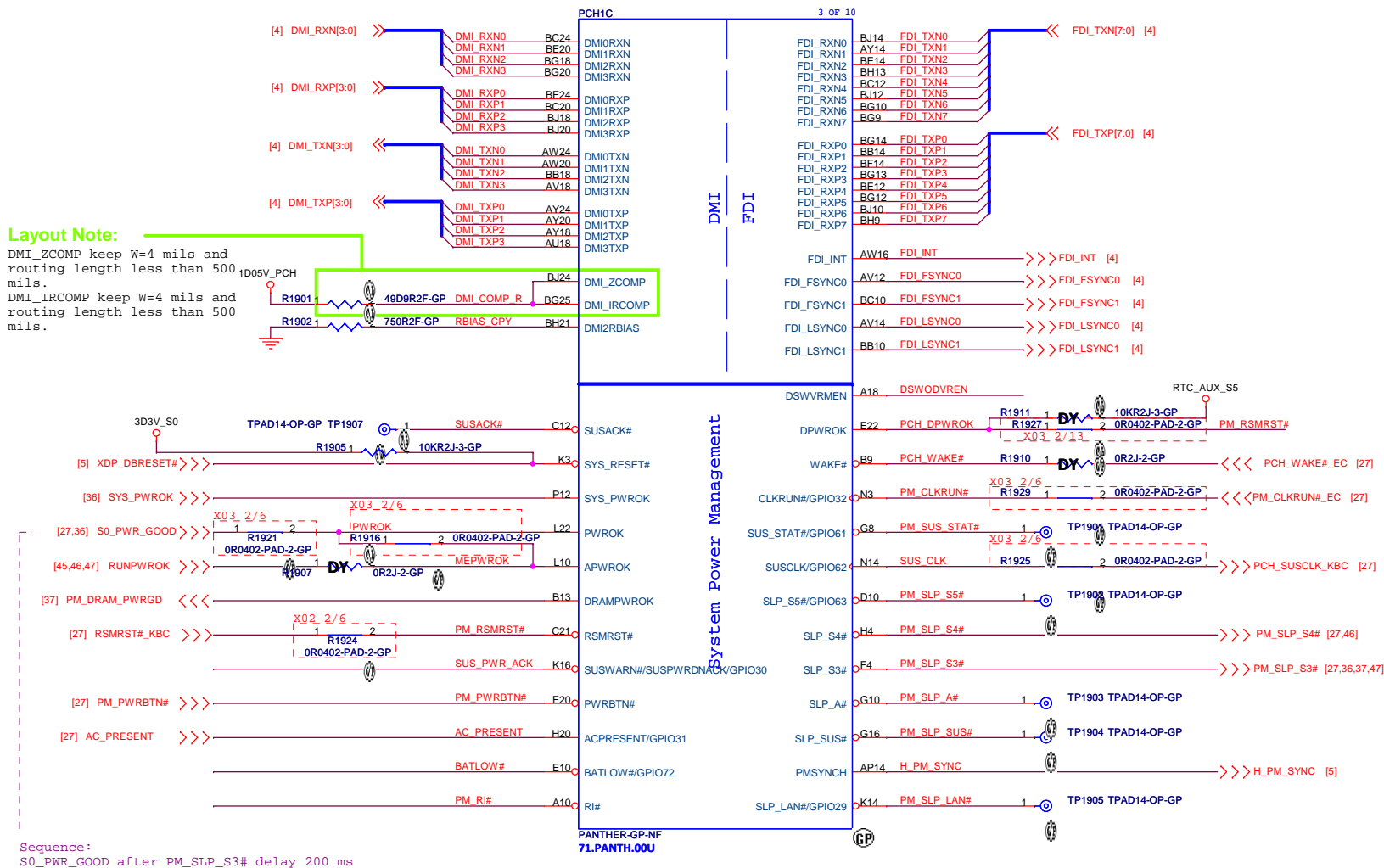
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Layout Note:

```
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.
```



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PCH (DM I/FDI/PM)

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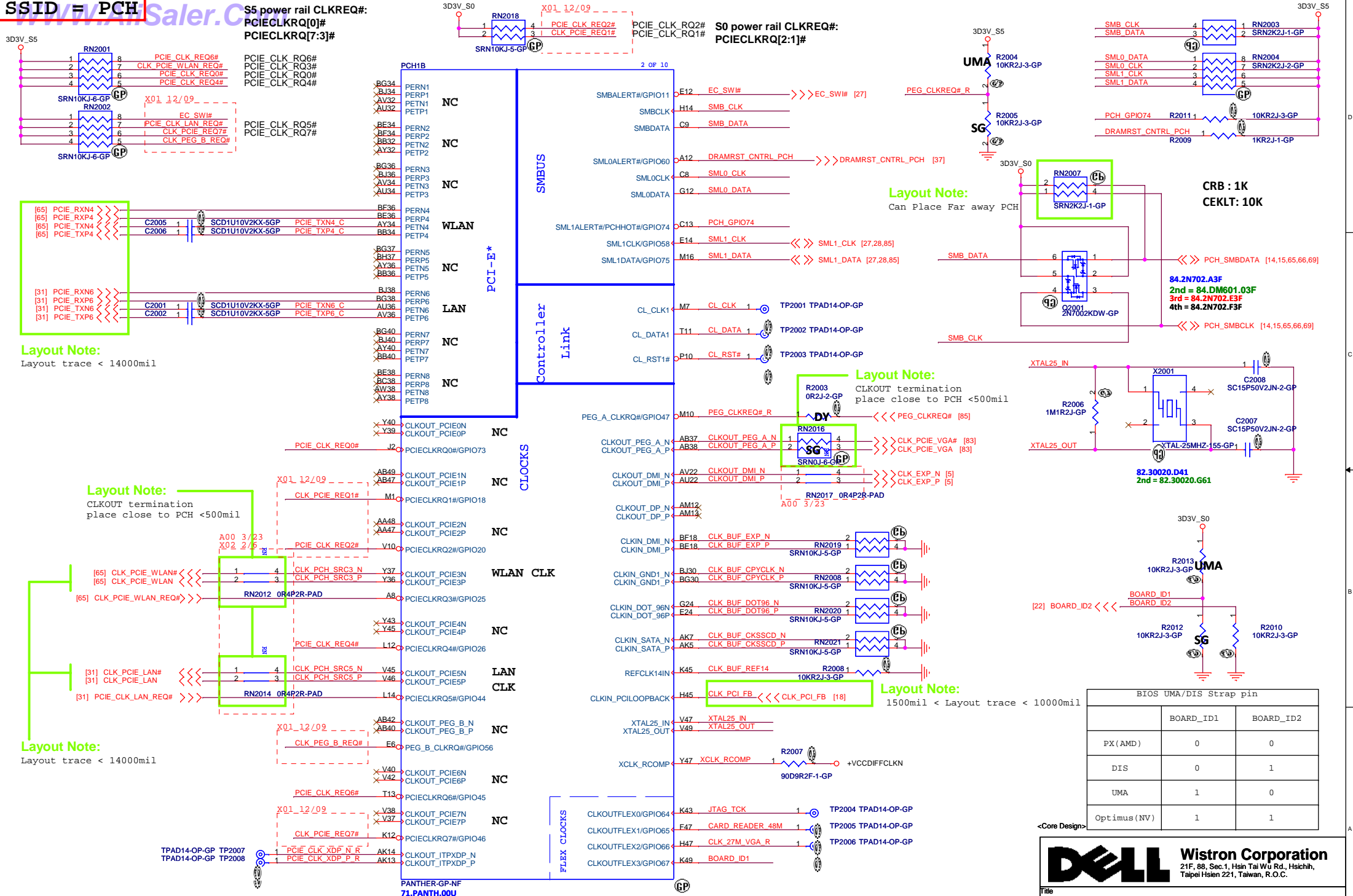
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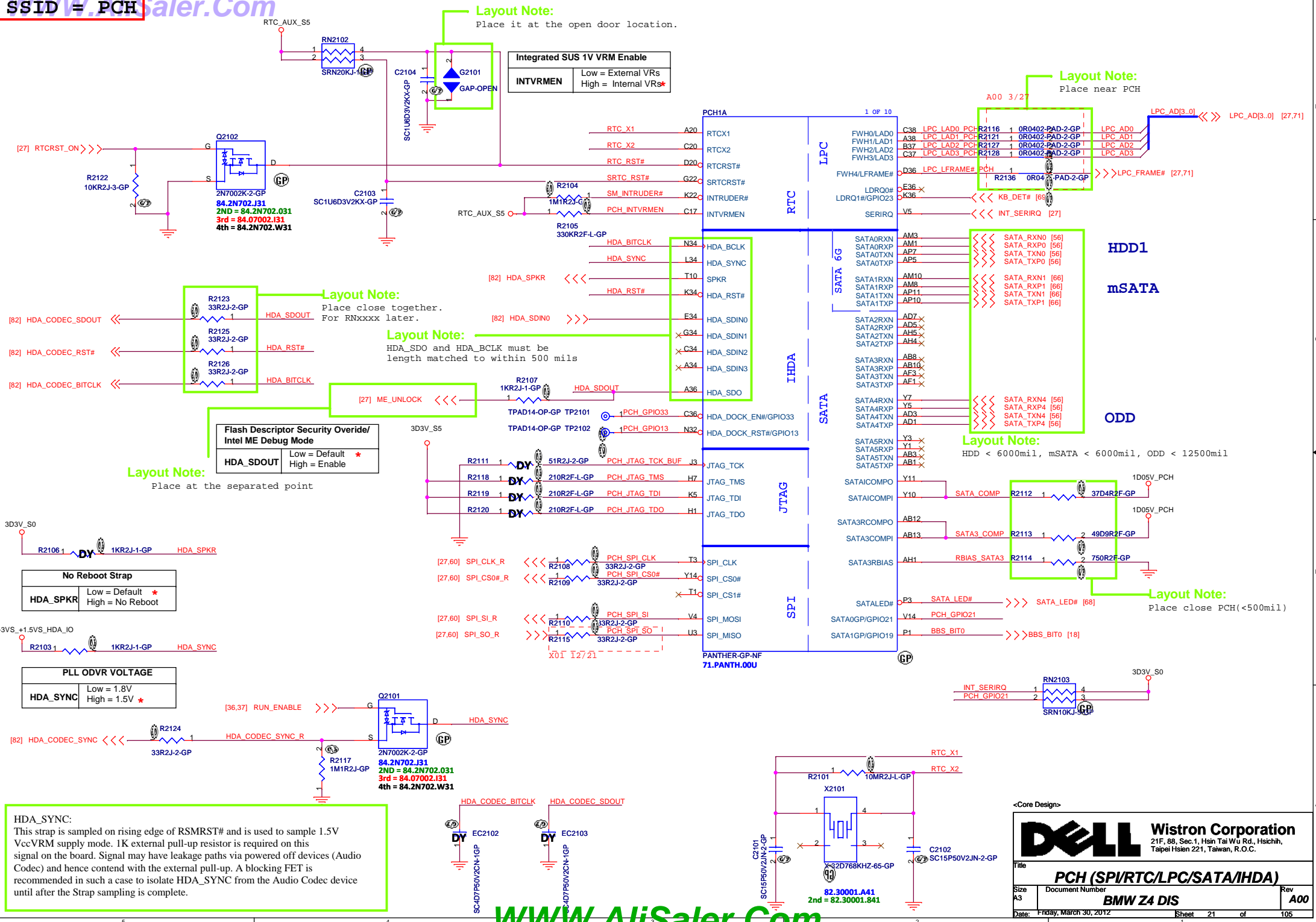
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-----	------------

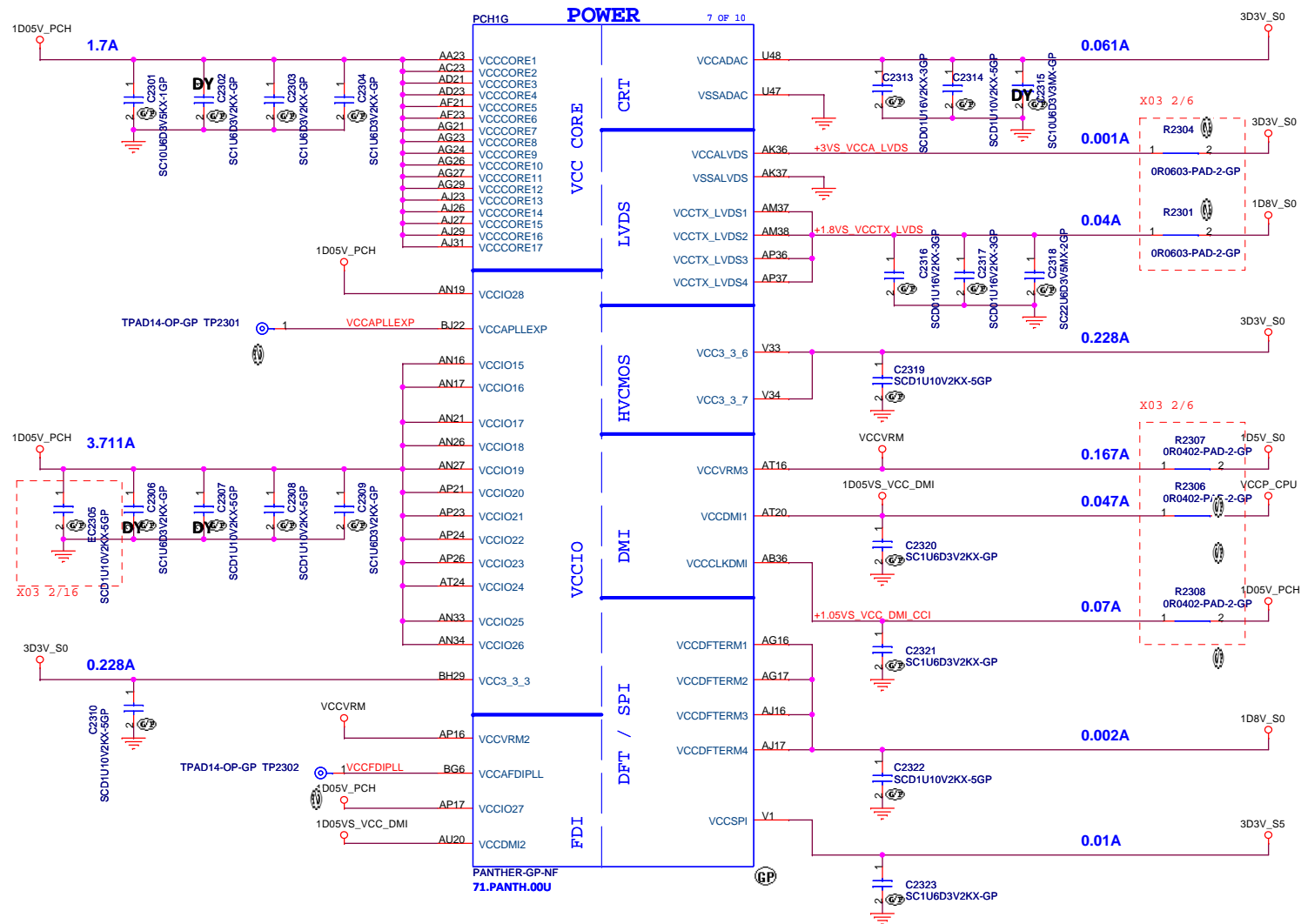
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S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:3]#







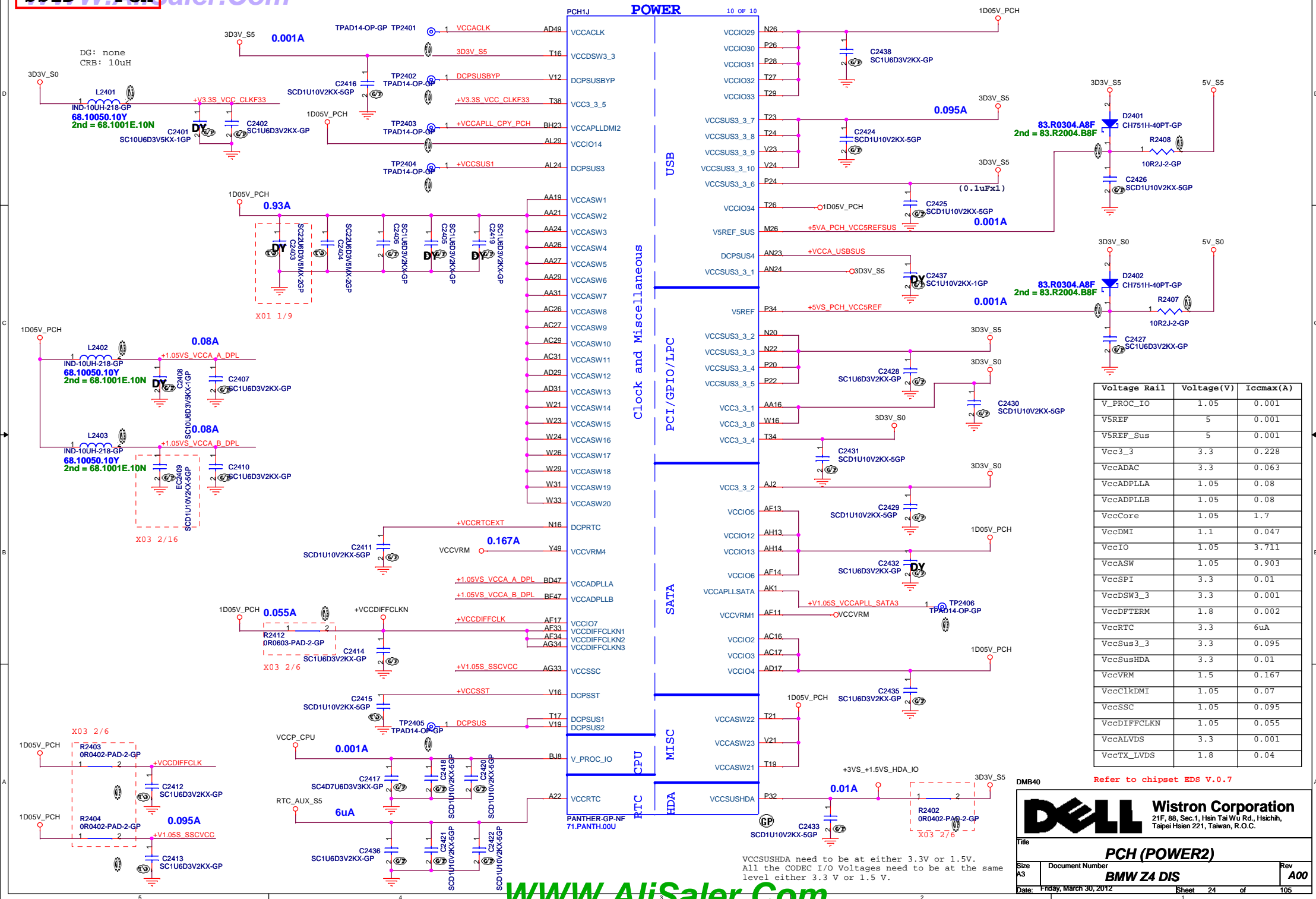
Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.0.7

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Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_I0	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADFLLA	1.05	0.08
VccADFLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.0.7



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PCH (POWER2)			
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PCH1H			8 OF 10
H5	VSS0		
AA17	VSS1	VSS80	AK38
AA2	VSS2	VSS81	AK4
AA3	VSS3	VSS82	AK42
AA33	VSS4	VSS83	AK46
AA34	VSS5	VSS84	AK8
AB11	VSS6	VSS85	AL16
AB14	VSS7	VSS86	AL17
AB39	VSS8	VSS87	AL19
AB4	VSS9	VSS88	AL2
AB43	VSS10	VSS89	AL21
AB5	VSS11	VSS90	AL23
AB7	VSS12	VSS91	AL26
AC19	VSS13	VSS92	AL27
AC2	VSS14	VSS93	AL31
AC21	VSS15	VSS94	AL33
AC24	VSS16	VSS95	AL34
AC33	VSS17	VSS96	AL48
AC34	VSS18	VSS97	AM11
AC48	VSS19	VSS98	AM14
AD10	VSS20	VSS99	AM36
AD11	VSS21	VSS100	AM39
AD12	VSS22	VSS101	AM43
AD13	VSS23	VSS102	AM45
AD19	VSS24	VSS103	AM46
AD24	VSS25	AM7	
AD26	VSS26	VSS104	AN2
AD27	VSS27	VSS105	AN29
AD33	VSS28	VSS106	AN3
AD34	VSS29	VSS107	AN31
AD36	VSS30	VSS108	AP12
AD37	VSS31	VSS109	AP19
AD38	VSS32	VSS110	AP28
AD39	VSS33	VSS111	AP30
AD4	VSS34	VSS112	AP32
AD40	VSS35	VSS113	AP38
AD42	VSS36	VSS114	AP4
AD43	VSS37	VSS115	AP42
AD45	VSS38	VSS116	AP46
AD46	VSS39	VSS117	AP8
AD8	VSS40	VSS118	AR2
AE2	VSS41	VSS119	AR48
AE3	VSS42	VSS120	AT11
AE10	VSS43	VSS121	AT13
AE12	VSS44	VSS122	AT18
AD14	VSS45	VSS123	AT22
AD16	VSS46	VSS124	AT26
AE16	VSS47	VSS125	AT28
AF19	VSS48	VSS126	AT30
AF24	VSS49	VSS127	AT32
AF26	VSS50	VSS128	AT34
AF27	VSS51	VSS129	AT39
AF29	VSS52	VSS130	AT42
AF31	VSS53	VSS131	AT46
AF38	VSS54	VSS132	AT7
AF4	VSS55	VSS133	AT7
AF42	VSS56	VSS134	AU24
AF46	VSS57	VSS135	AU30
AF5	VSS58	VSS136	AU36
AF7	VSS59	VSS137	AV20
AF8	VSS60	VSS138	AV24
AG19	VSS61	VSS139	AV30
AG2	VSS62	VSS140	AV38
AG31	VSS63	VSS141	AV4
AG48	VSS64	VSS142	AV43
AH11	VSS65	VSS143	AV8
AH3	VSS66	VSS144	AW14
AH36	VSS67	VSS145	AW18
AH39	VSS68	VSS146	AW2
AH40	VSS69	VSS147	AW22
AH42	VSS70	VSS148	AW26
AH46	VSS71	VSS149	AW28
AH7	VSS72	VSS150	AW34
AJ19	VSS73	VSS151	AW36
AJ21	VSS74	VSS152	AW40
AJ24	VSS75	VSS153	AW48
AJ33	VSS76	VSS154	AW48
AJ34	VSS77	VSS155	AV11
AK12	VSS78	VSS156	AY12
AK3	VSS79	VSS157	AY22
		VSS158	AY28

PANTHER-GP-NF
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PCH1I			9 OF 10
AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
AY8	VSS162	VSS262	K39
B11	VSS163	VSS263	K46
B15	VSS164	VSS264	K7
B19	VSS165	VSS265	L18
B23	VSS166	VSS266	L2
B27	VSS167	VSS267	L20
B31	VSS168	VSS268	L26
B35	VSS169	VSS269	L28
B39	VSS170	VSS270	L36
B7	VSS171	VSS271	L48
F45	VSS172	VSS272	M12
BB12	VSS173	VSS273	P16
BB16	VSS174	VSS274	M18
BB20	VSS175	VSS275	M22
BB22	VSS176	VSS276	M24
BB24	VSS177	VSS277	M30
BB28	VSS178	VSS278	M32
BB30	VSS179	VSS279	M34
BB38	VSS180	VSS280	M38
BB4	VSS181	VSS281	M4
BB46	VSS182	VSS282	M42
BC14	VSS183	VSS283	M46
BC18	VSS184	VSS284	M8
BC2	VSS185	VSS285	N18
BC22	VSS186	VSS286	P30
BC26	VSS187	VSS287	N47
BC32	VSS188	VSS288	P11
BC34	VSS189	VSS289	P18
BC36	VSS190	VSS290	T33
BC40	VSS191	VSS291	P40
BC42	VSS192	VSS292	P43
BC48	VSS193	VSS293	P47
BD46	VSS194	VSS294	P7
BD5	VSS195	VSS295	R2
BE22	VSS196	VSS296	R48
BE26	VSS197	VSS297	T12
BE40	VSS198	VSS298	T31
BF10	VSS199	VSS299	T37
BF12	VSS200	VSS300	T4
BF16	VSS201	VSS301	W34
BF20	VSS202	VSS302	T46
BF22	VSS203	VSS303	T47
BF24	VSS204	VSS304	T8
BF26	VSS205	VSS305	V11
BF28	VSS206	VSS306	V17
BF3	VSS207	VSS307	V26
BF30	VSS208	VSS308	V27
BF38	VSS209	VSS309	V29
BF40	VSS210	VSS310	V31
BF8	VSS211	VSS311	V36
BG17	VSS212	VSS312	V39
BG21	VSS213	VSS313	V43
BG33	VSS214	VSS314	V7
BG44	VSS215	VSS315	W17
BG8	VSS216	VSS316	W19
BH11	VSS217	VSS317	W2
BH15	VSS218	VSS318	W27
BH17	VSS219	VSS319	W48
BH19	VSS220	VSS320	Y12
H10	VSS221	VSS321	Y38
BH27	VSS222	VSS322	Y4
BH31	VSS223	VSS323	Y42
BH33	VSS224	VSS324	Y46
BH35	VSS225	VSS325	Y8
BH39	VSS226	VSS326	BG29
BH43	VSS227	VSS327	N24
BH7	VSS228	VSS328	AJ3
D3	VSS229	VSS329	AD47
D12	VSS230	VSS330	B43
D16	VSS231	VSS331	BE10
D18	VSS232	VSS332	BG41
D22	VSS233	VSS333	G14
D24	VSS234	VSS334	H16
D26	VSS235	VSS335	T36
D30	VSS236	VSS336	BG22
D32	VSS237	VSS337	BG24
D34	VSS238	VSS338	C22
D38	VSS239	VSS339	AP13
D42	VSS240	VSS340	M14
D4	VSS241	VSS341	AP3
E18	VSS242	VSS342	AP1
E26	VSS243	VSS343	BE16
G18	VSS244	VSS344	BC16
G20	VSS245	VSS345	BG28
G26	VSS246	VSS346	BG28
G28	VSS247	VSS347	BJ28
G36	VSS248	VSS348	
G48	VSS249	VSS349	
H12	VSS250	VSS350	
H18	VSS251	VSS351	
H22	VSS252	VSS352	
H24	VSS253		
H26	VSS254		
H30	VSS255		
H32	VSS256		
H34	VSS257		
F3	VSS258		

PANTHER-GP-NF
71.PANTH.00U



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Title			PCH (VSS)	
Size	Document Number	Rev		
A3	BMW Z4 DIS	A00		
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

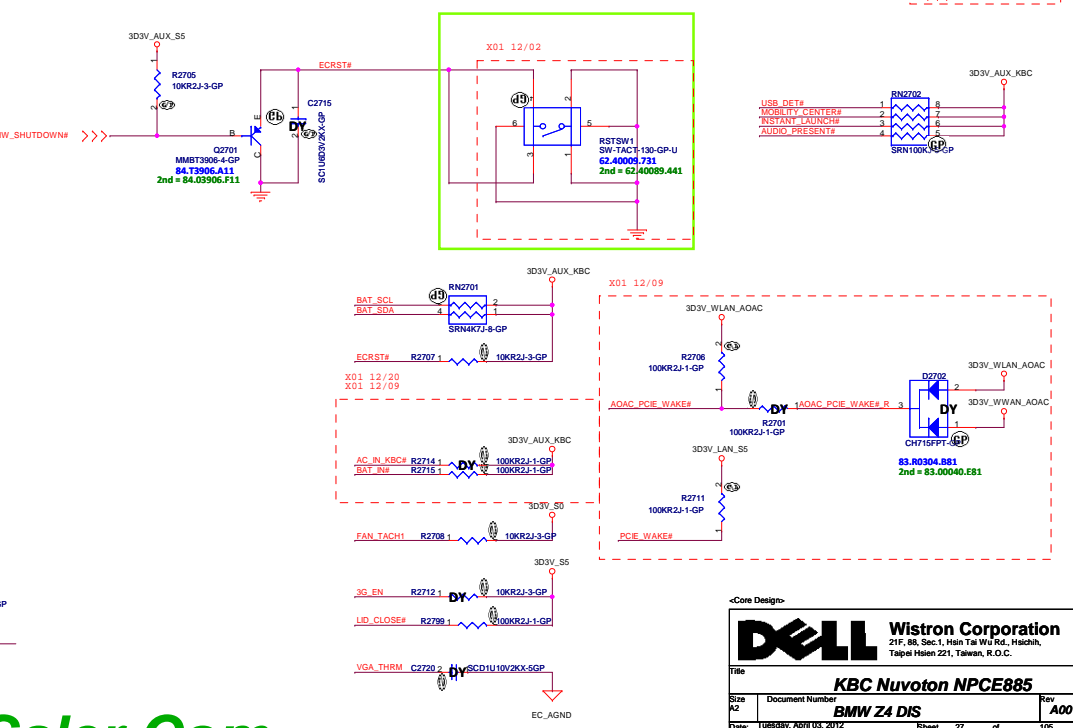
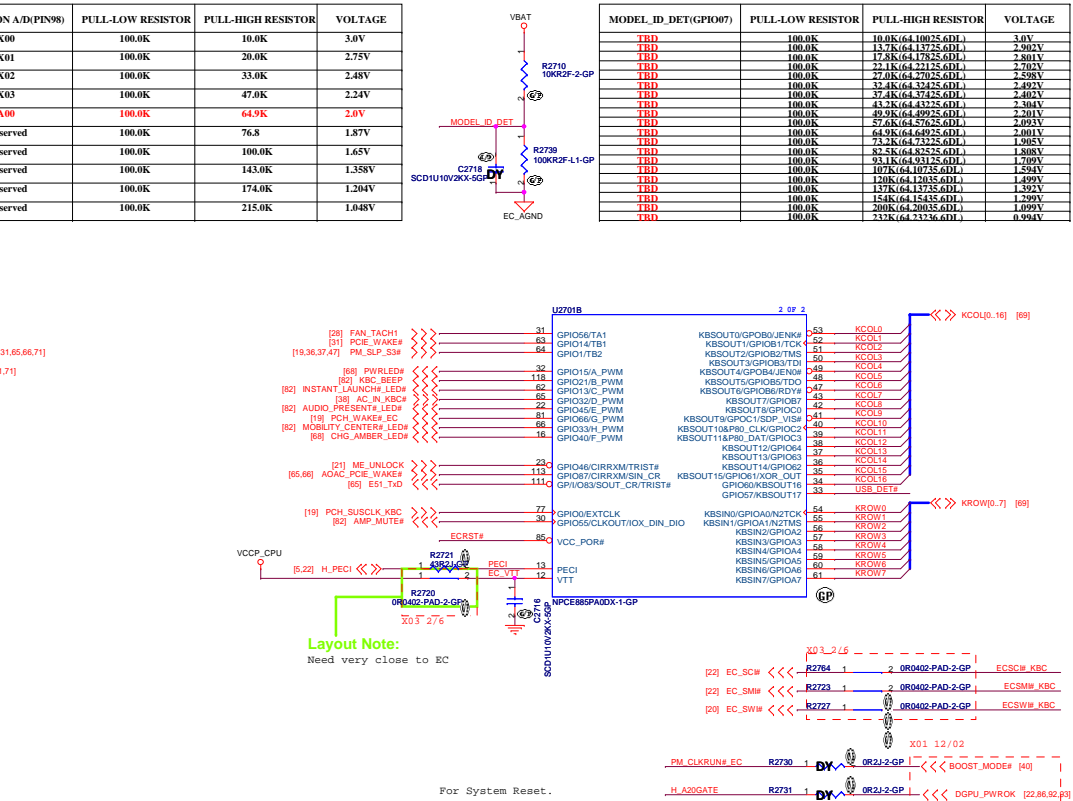
Document Number
BMW Z4 DIS

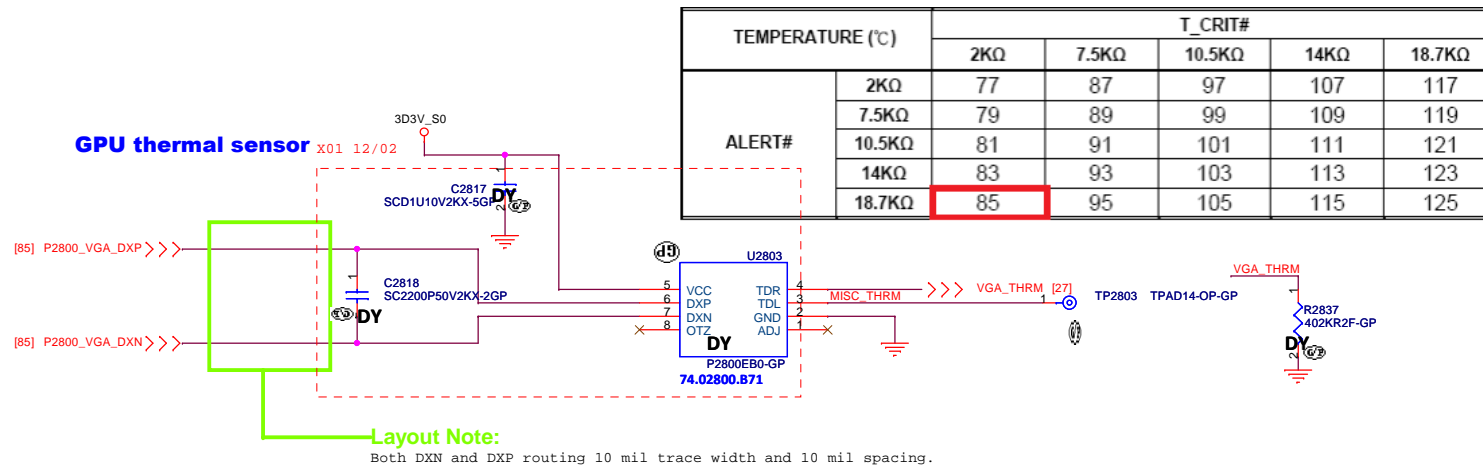
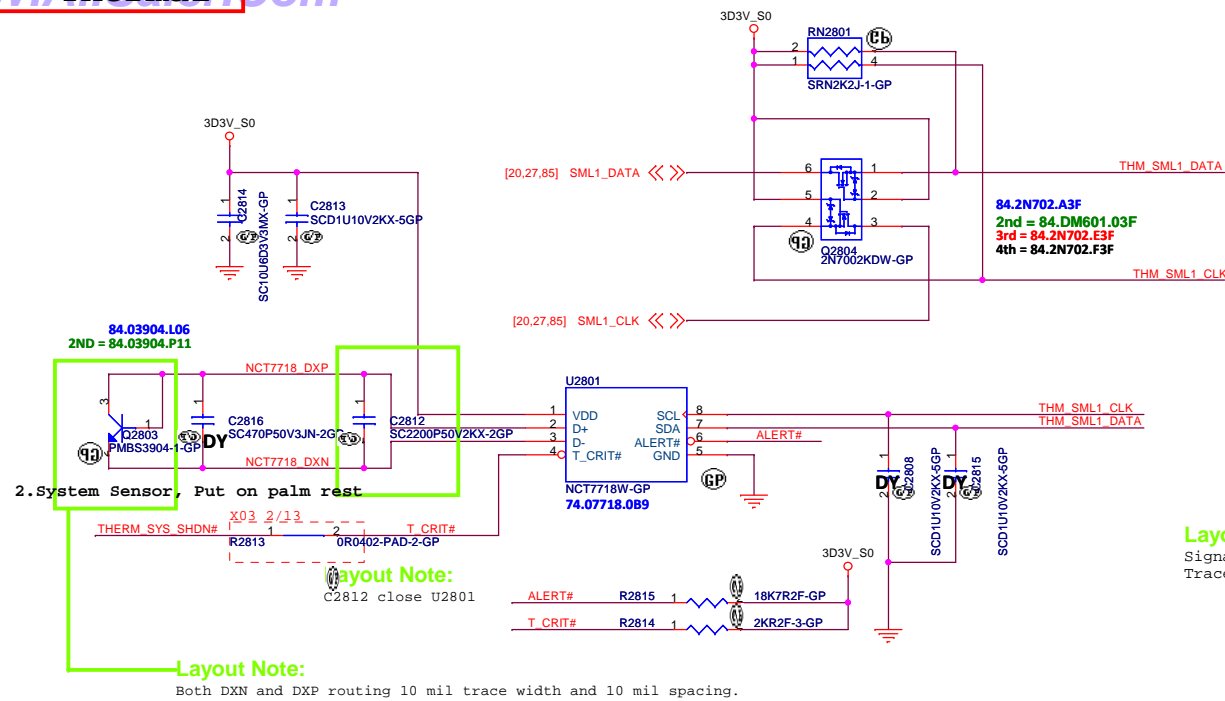
Date: Friday, March 30, 2012

Rev
A00

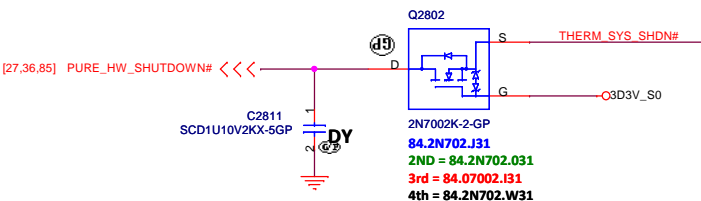
Sheet 26 of 105

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
TBD	100.0K	10.0K (6.10025 ADJ.)	3.6V
TBD	100.0K	12.7K (6.1375 ADJ.)	3.903V
TBD	100.0K	17.8K (6.17875 ADJ.)	2.801V
TBD	100.0K	21.1K (6.22125 ADJ.)	2.702V
TBD	100.0K	27.0K (6.27025 ADJ.)	2.598V
TBD	100.0K	32.4K (6.32425 ADJ.)	2.492V
TBD	100.0K	37.4K (6.37425 ADJ.)	2.403V
TBD	100.0K	43.2K (6.43275 ADJ.)	2.304V
TBD	100.0K	49.9K (6.49925 ADJ.)	2.201V
TBD	100.0K	57.6K (6.57625 ADJ.)	2.093V
TBD	100.0K	64.9K (6.64925 ADJ.)	2.001V
TBD	100.0K	72.7K (6.72725 ADJ.)	1.903V
TBD	100.0K	82.6K (6.82625 ADJ.)	1.808V
TBD	100.0K	93.1K (6.93125 ADJ.)	1.709V
TBD	100.0K	107.5K (6.1075 ADJ.)	1.604V
TBD	100.0K	120K (6.1205 ADJ.)	1.499V
TBD	100.0K	137K (6.1375 ADJ.)	1.393V
TBD	100.0K	154K (6.1545 ADJ.)	1.299V
TBD	100.0K	200K (6.2005 ADJ.)	1.099V
TBD	100.0K	328K (6.328 ADJ.)	0.699V





Thermal Sensor	
ADJ	Temp. (C)
Pull high	95
Pull low	90
Floating	85



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Title Reserved			
Size A3	Document Number BMW Z4 DIS		Rev A00
Date: Friday, March 30, 2012	Sheet	29	of 105

(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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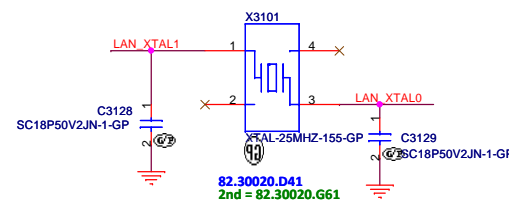
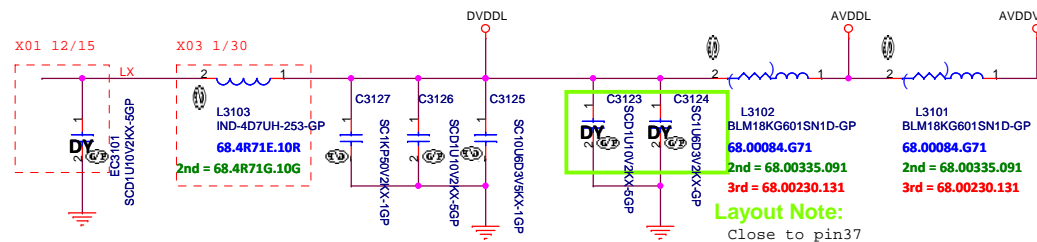
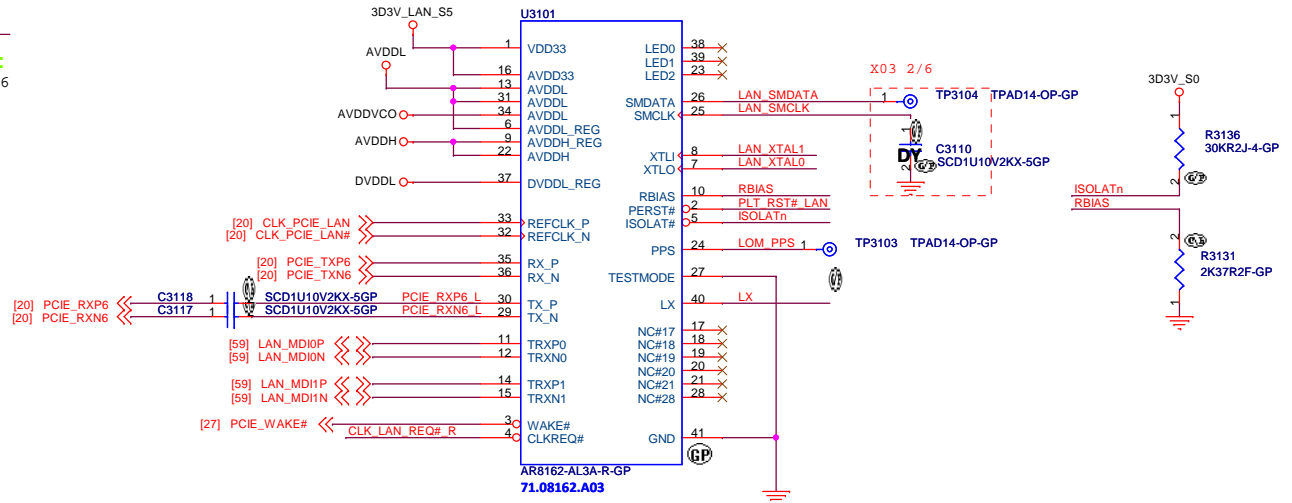
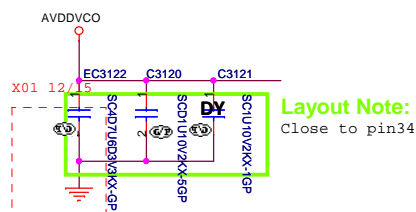
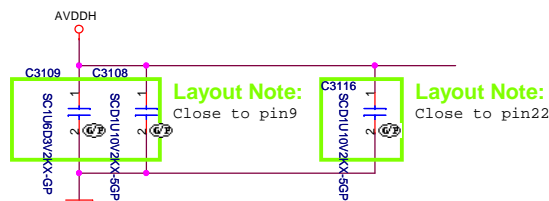
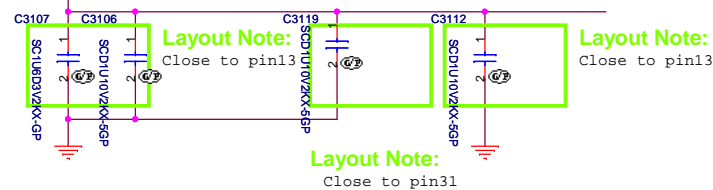
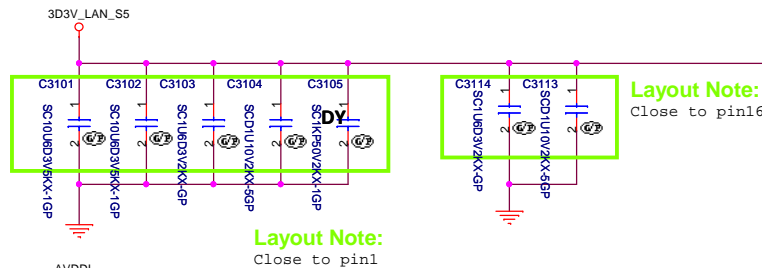
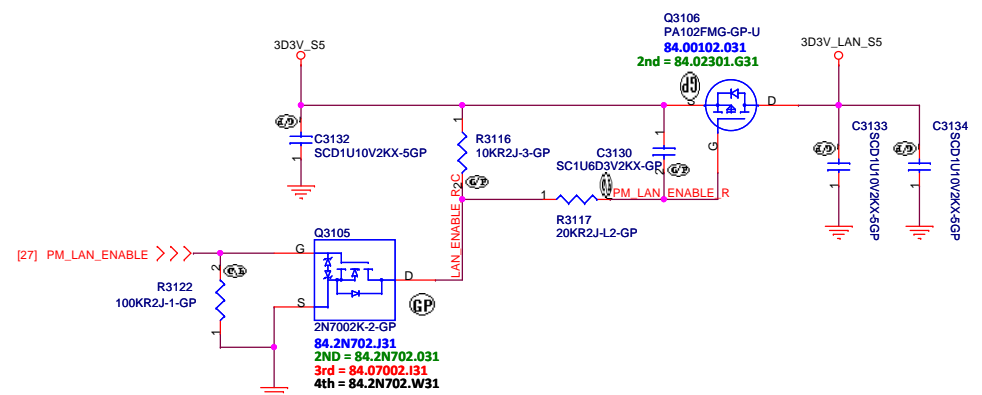
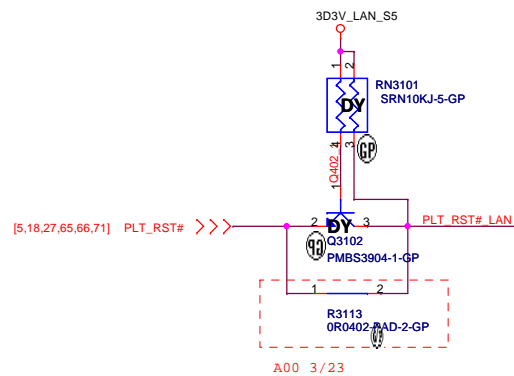
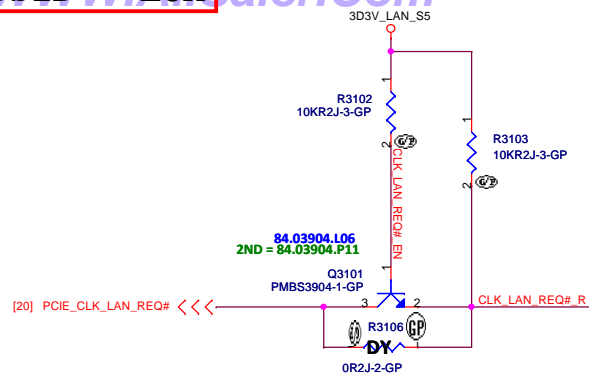
Size
A3

Document Number
BMW Z4 DIS

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Date: Friday, March 30, 2012

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(Blanking)

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A3

Document Number

Date: Friday, March 30, 2012


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(Blanking)

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Reserved

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Title

Reserved

Size
A3

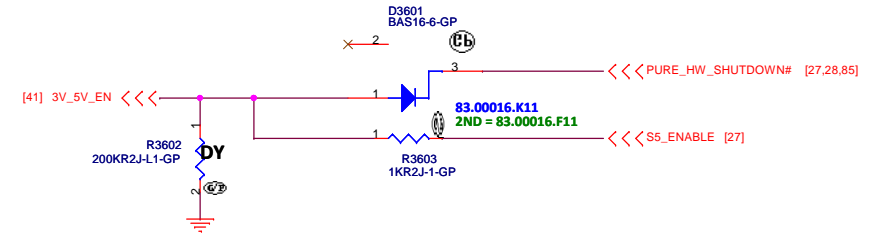
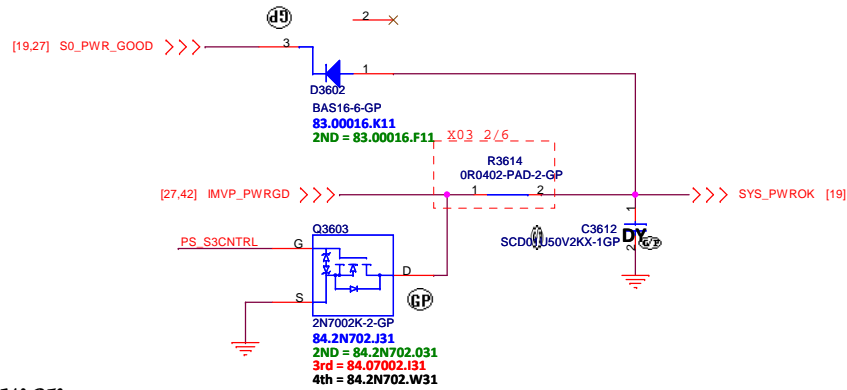
Document Number
BMW Z4 DIS

Rev
A00

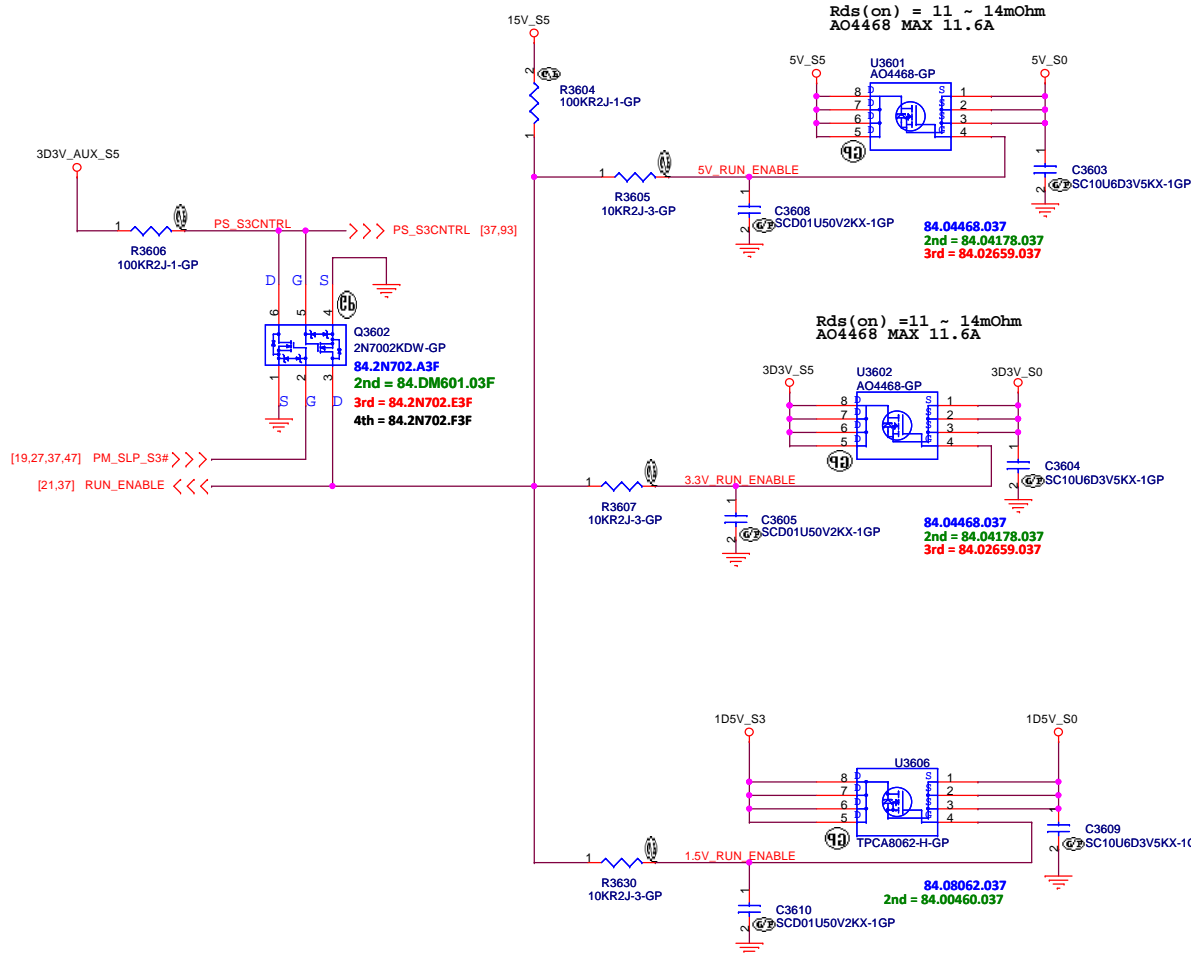
Date: Friday, March 30, 2012

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SSID = Reset.Suspend

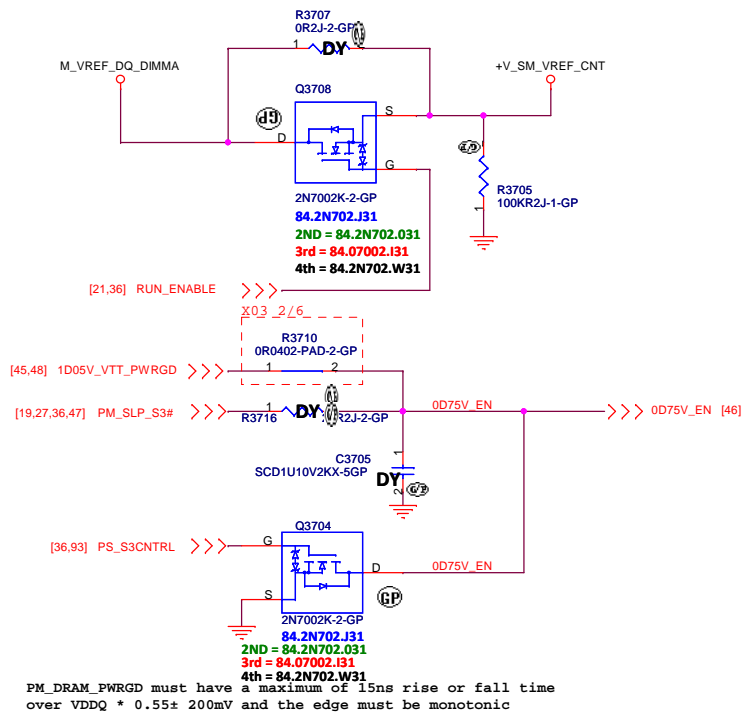


ROSA Run Power

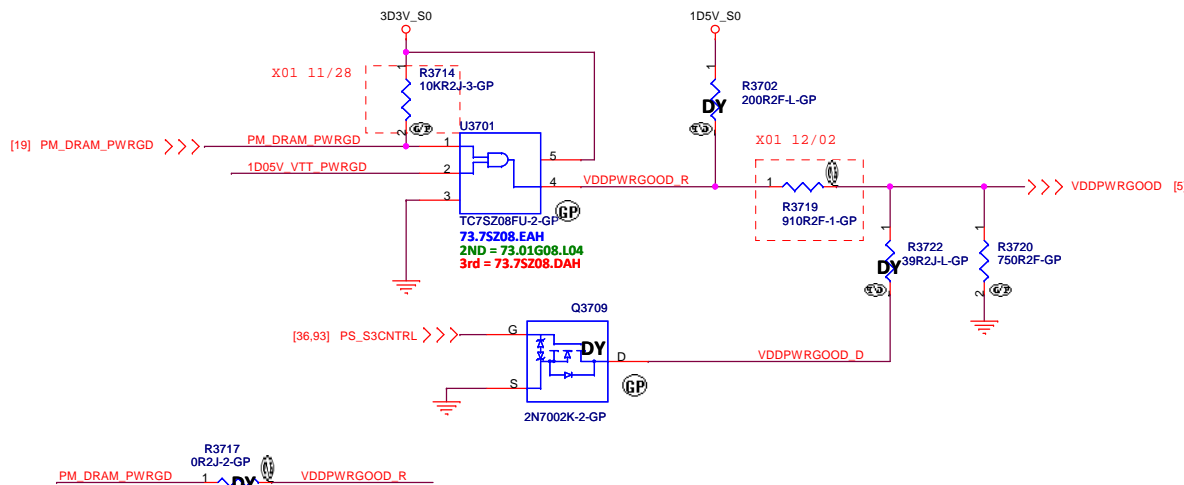


SSID = Reset.Suspend

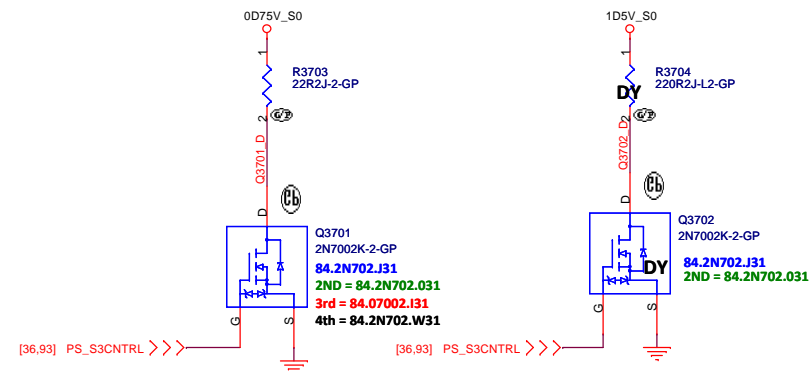
Close to CPU S3 Power Reduction Circuit Processor VREF_DQ Implementation



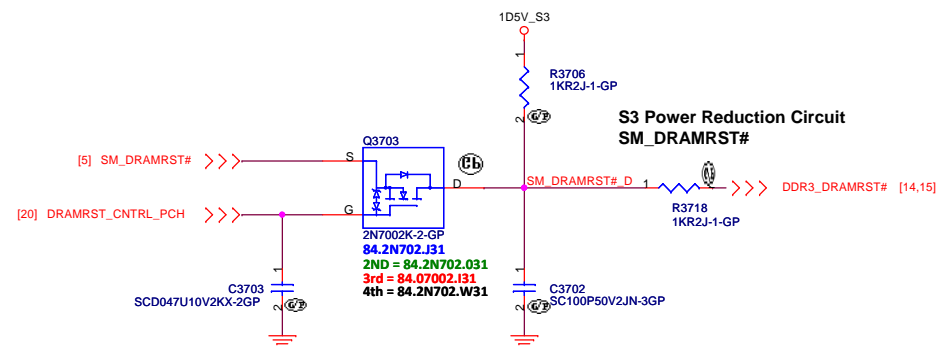
Close to CPU S3 Power Reduction Circuit PM_DRAM_PWRGD



Close to DIMM S3 Power Reduction Circuit PM_DRAM_PWRGD



Close to CPU S3 Power Reduction Circuit SM_DRAMRST#

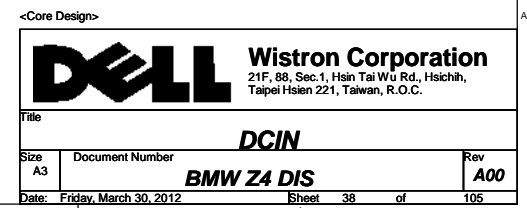


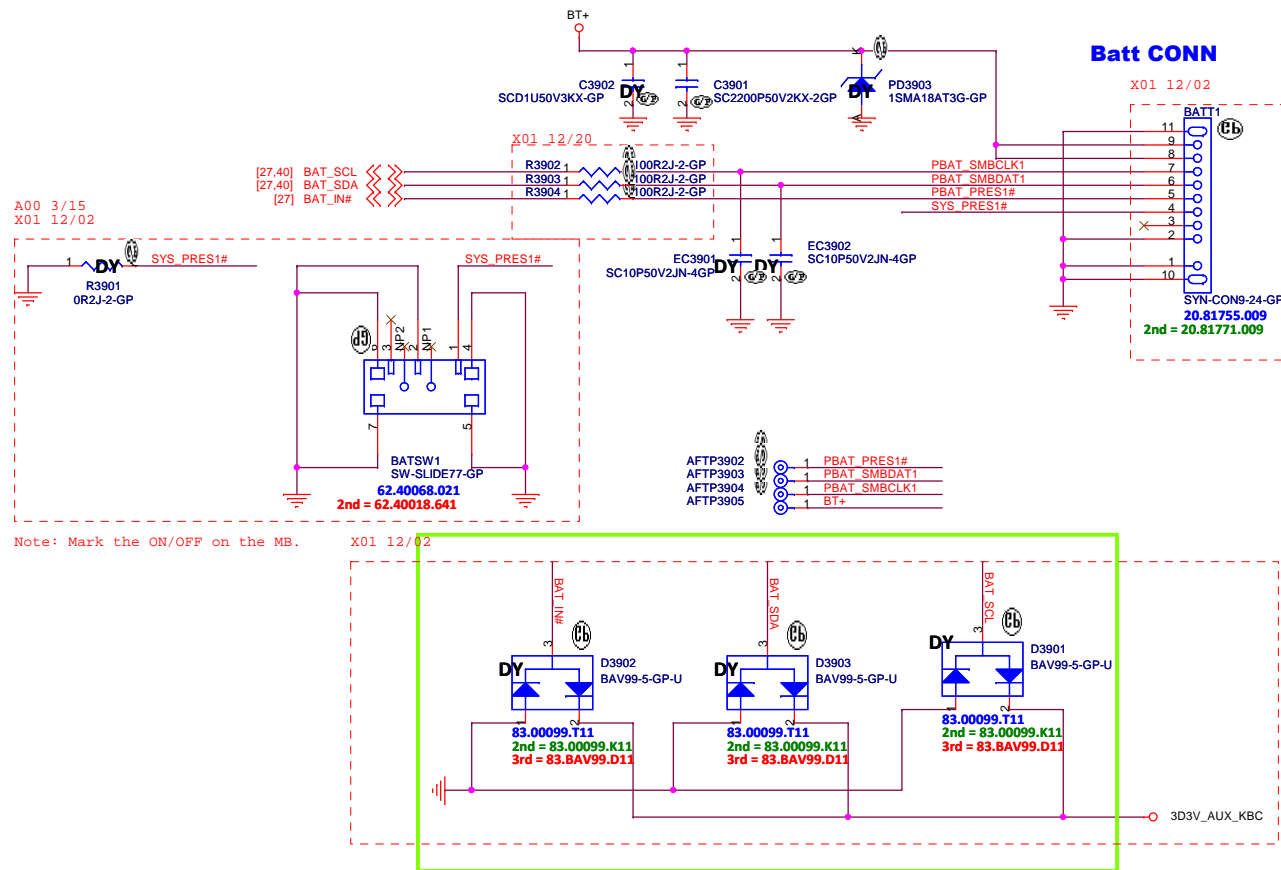
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Title			S3 Power Reduction	
Size			BMW Z4 DIS	
Date			Friday, March 30, 2012	Sheet 37 of 105





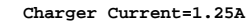
Layout Note:
Place near Battery CONN

<Core Design>

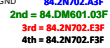


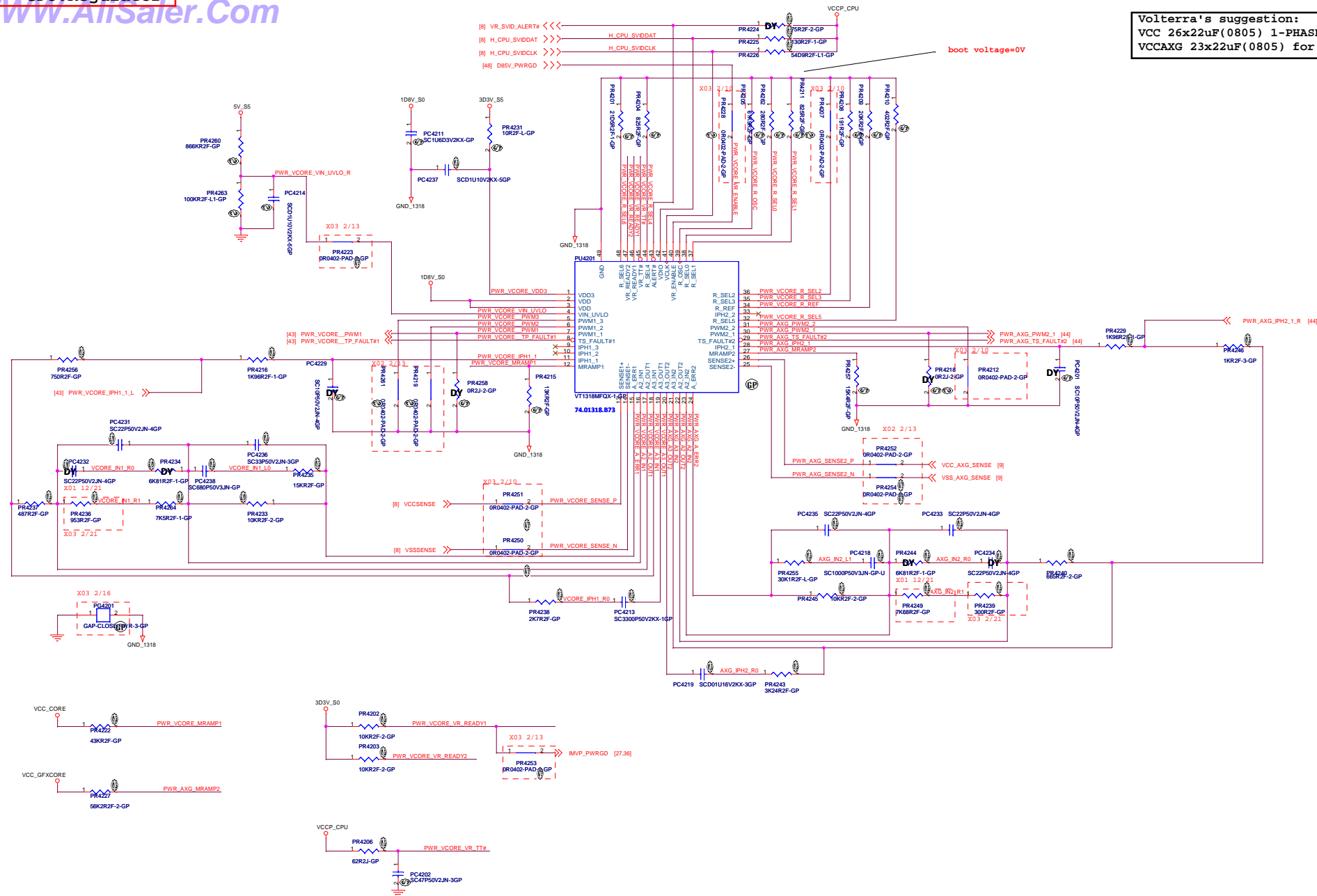
Wistron Corporation
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Title			BATT CONN	
Size	Document Number	Rev		
A3	BMW Z4 DIS	A00		
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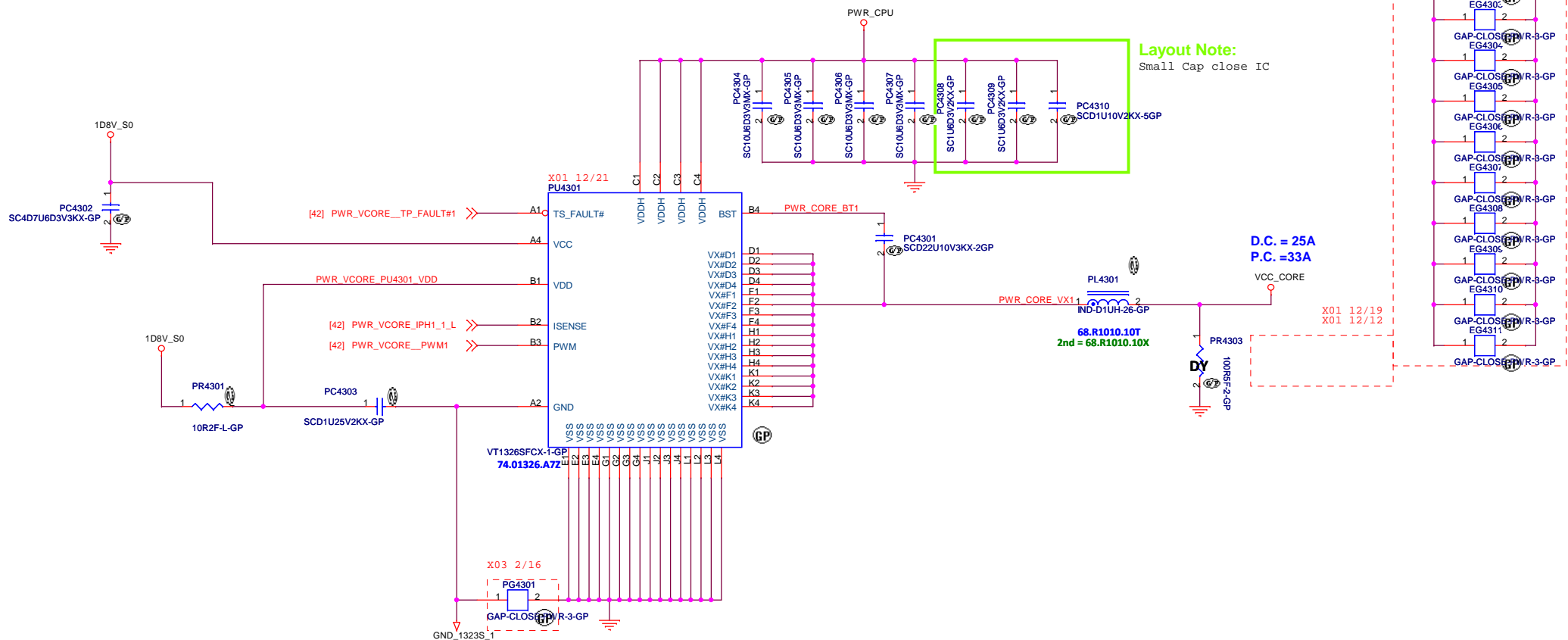
H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1





Volterra's suggestion: VCC 26x22uF(0805) 1-PHASE VCC VCCAXG 23x22uF(0805) for 1-PHASE VCCAXG
--

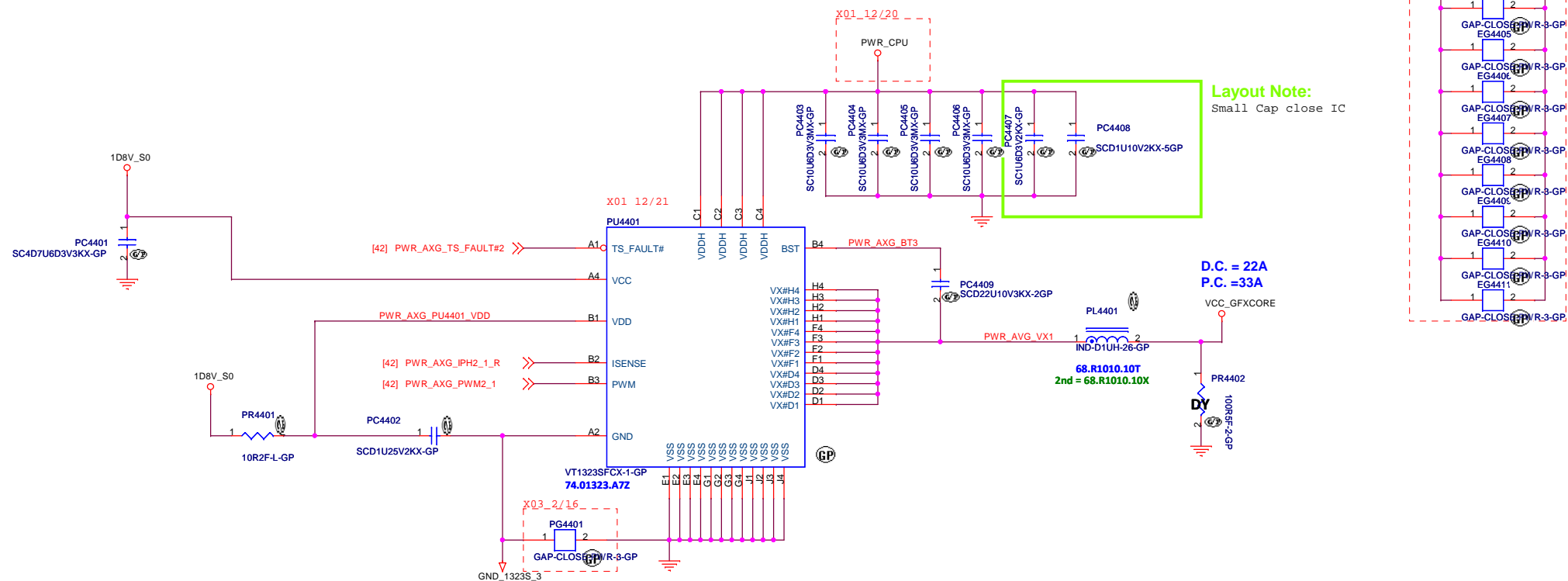
SSID = CPU.Regulator



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title VT1318+1326_CPU_CORE2+1(2/3)			
Size A3	Document Number	Rev A00	
BMW Z4 DIS			
Date: Friday, March 30, 2012	Sheet 43	of	105

```
SSID = CPU.Regulator
```



<Core Design>

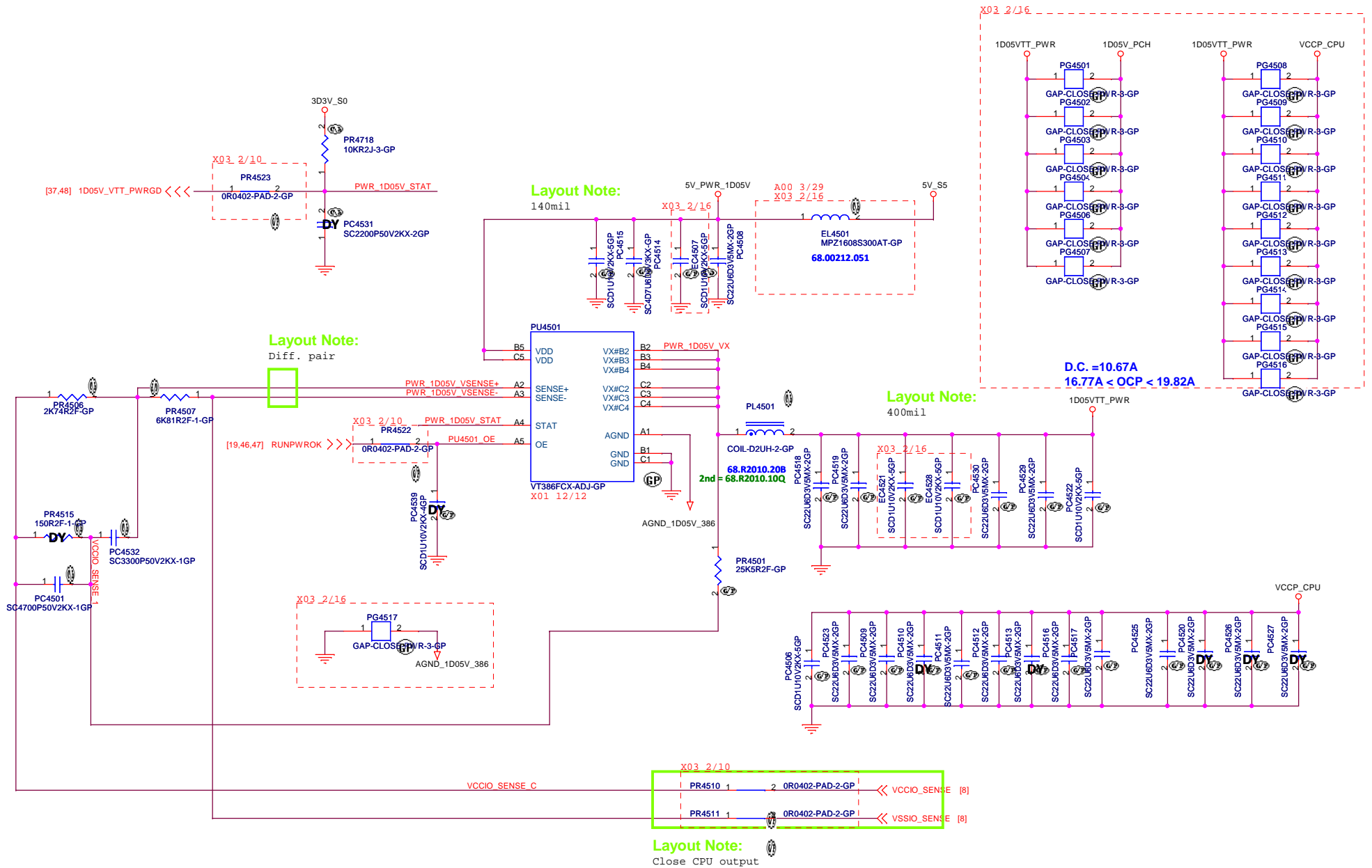


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Title			
VT1318+1323_CPU_CORE1+1(3/3)			
Size	Document Number	Rev	
A3	BMW Z4 DIS	A	
Date:	Friday, March 30, 2012	Sheet	44 of 105

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SSID = PWR.Plane.Regulator_1p05v



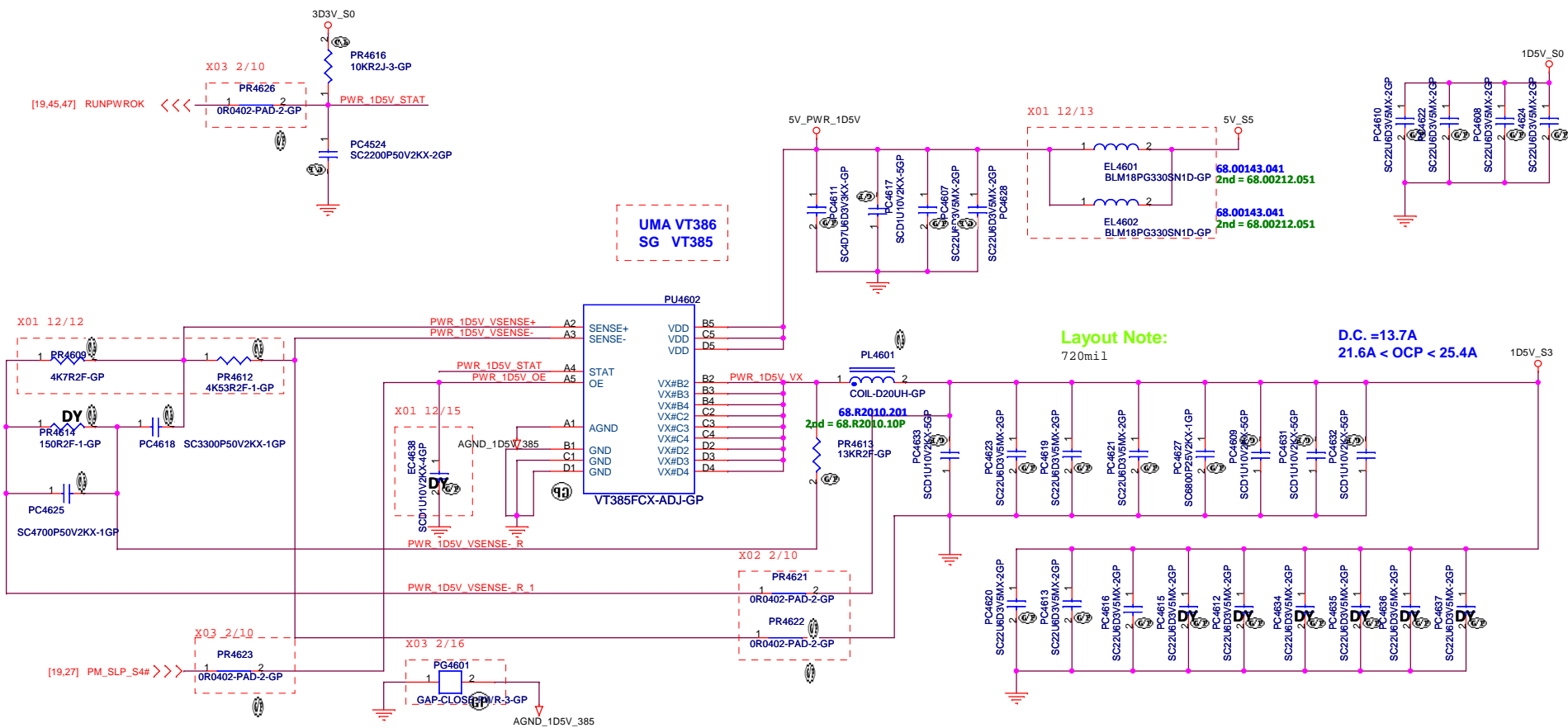
<Core Design>



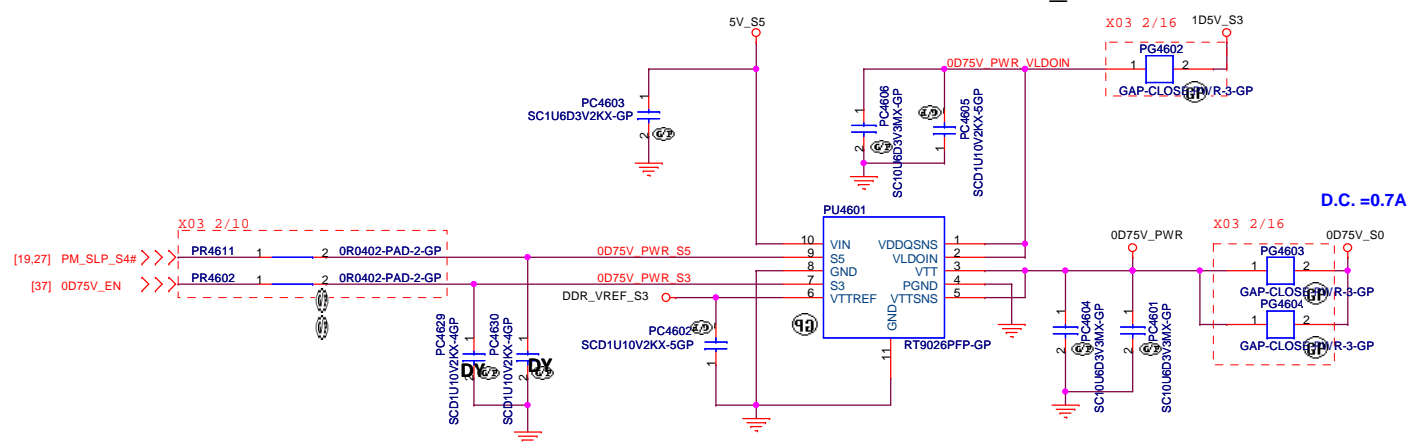
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title			1D05V PCH & VCCP CPU	
Size	Document Number	BMW Z4 DIS		Rev
A3				A00
Date: Friday, March 30, 2012		Sheet	45	of 105

```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



RT9026 for 0D75V_S0



<Core Design>

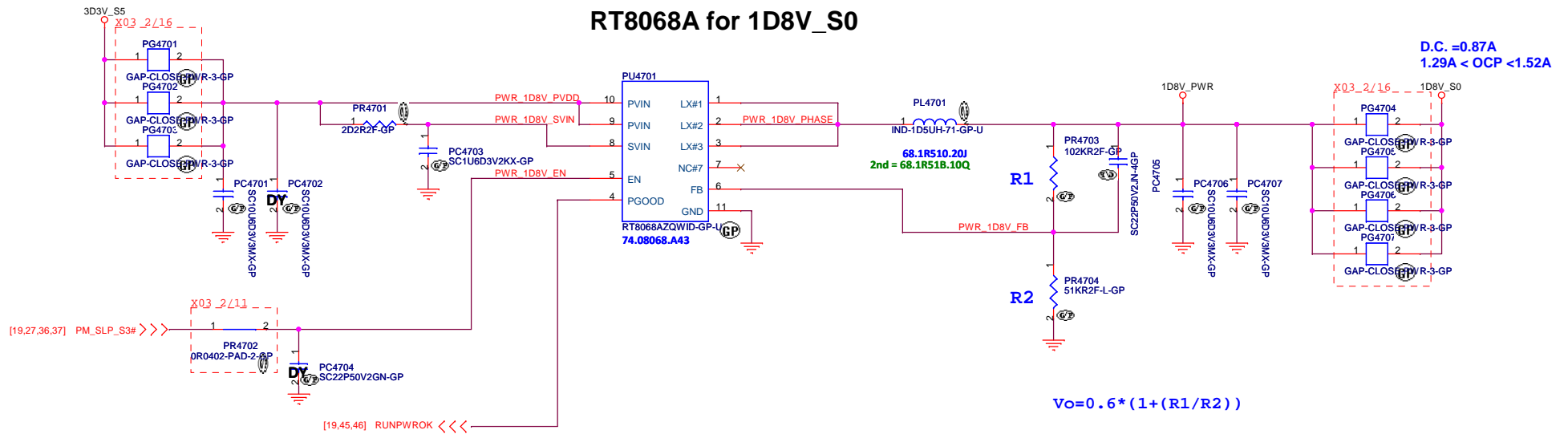


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Title			
VT385 1D5V S3/RT9026 0D75V S0			
Size A3	Document Number	Rev	
	BMW Z4 DIS	A00	
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SSID = PWR.Plane.Regulator_1p8v

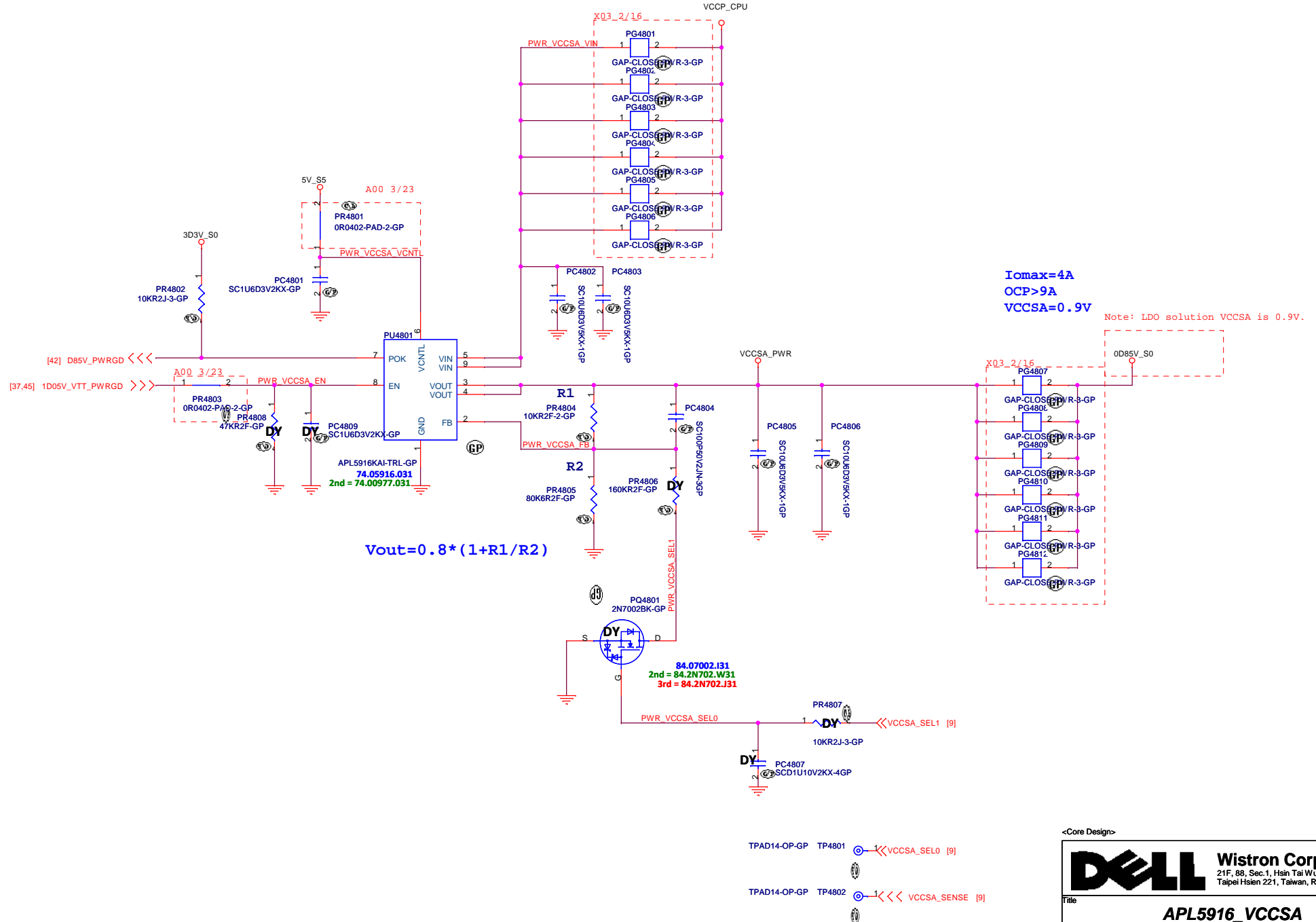


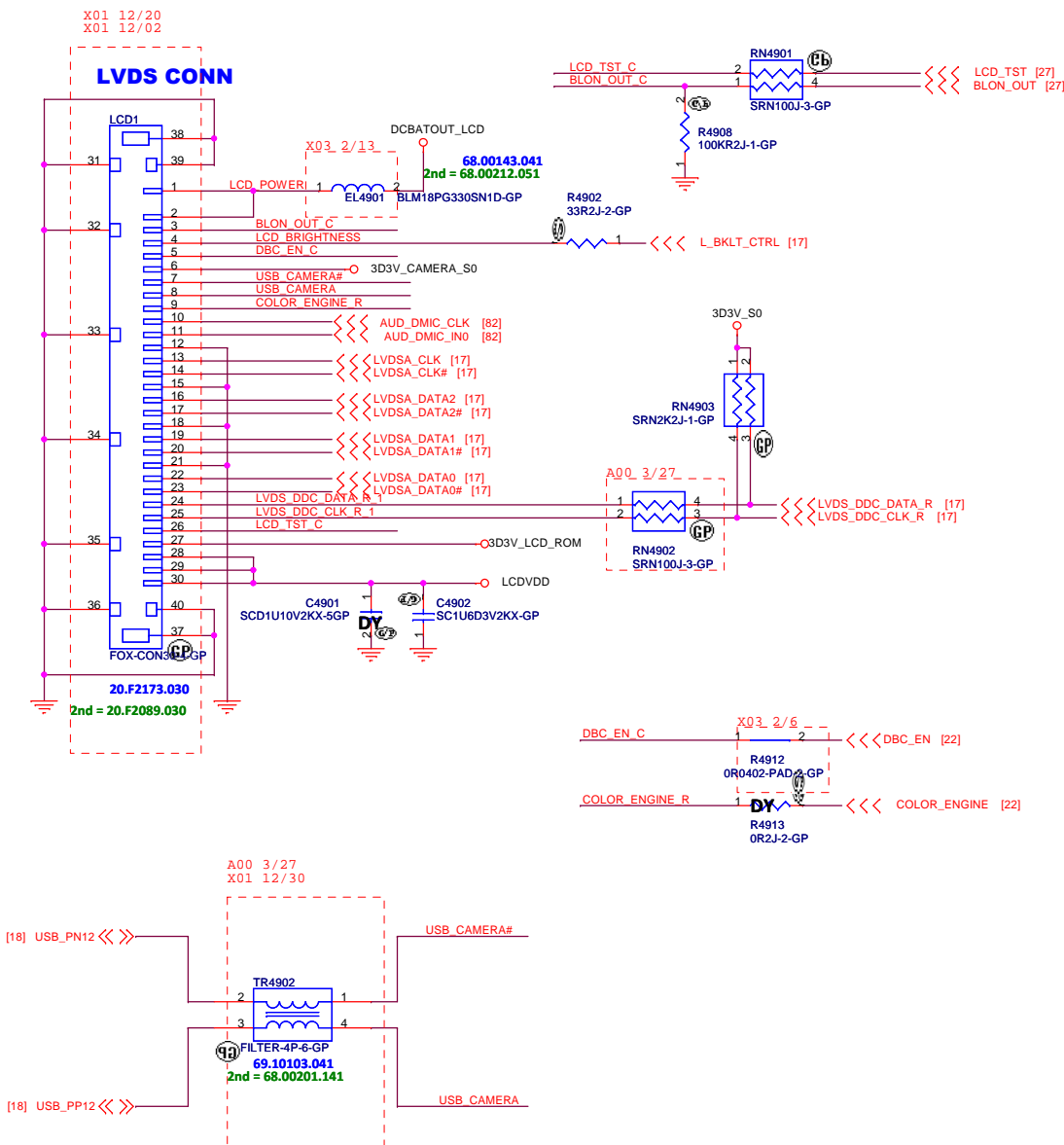
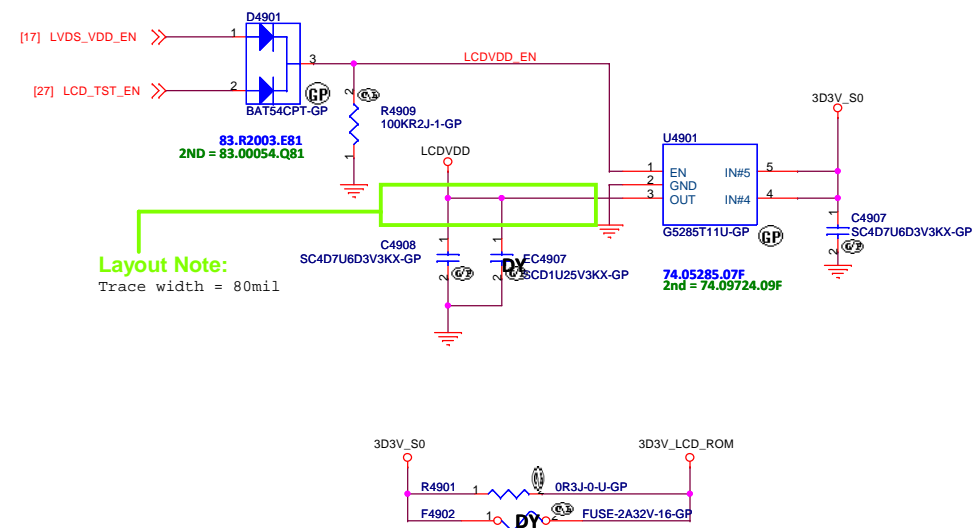
<Core Design>

DELL			Wistron Corporation		
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Title					
RT8068A 1D8V S0					
Size	Document Number				Rev
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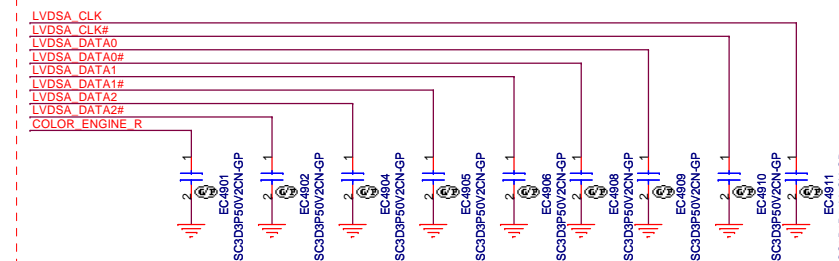
SSID = PWR.Plane.Regulator_vccsa

X02 1/9



**Camera Power****LCD Power for ROSA**

X03 2/16



<Core Design>




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LCD Connector			
Size A3	Document Number	Rev	
		BMW Z4 DIS	
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Title

CRT Connector

Size
A3

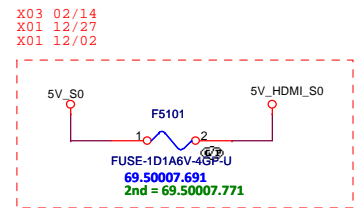
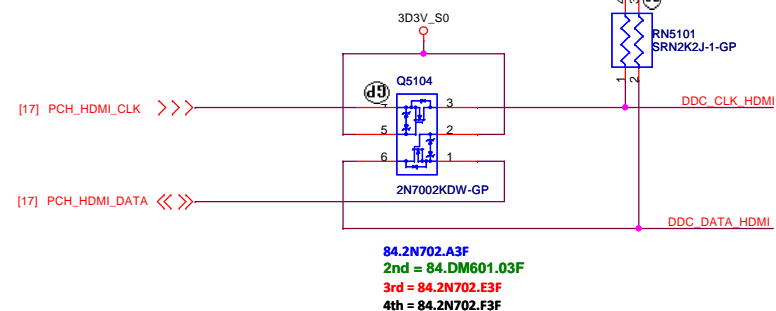
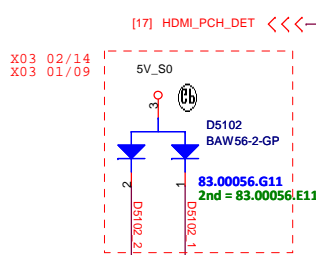
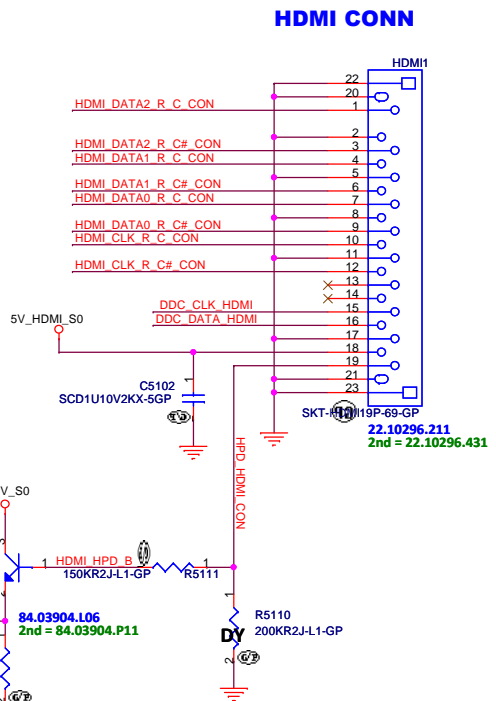
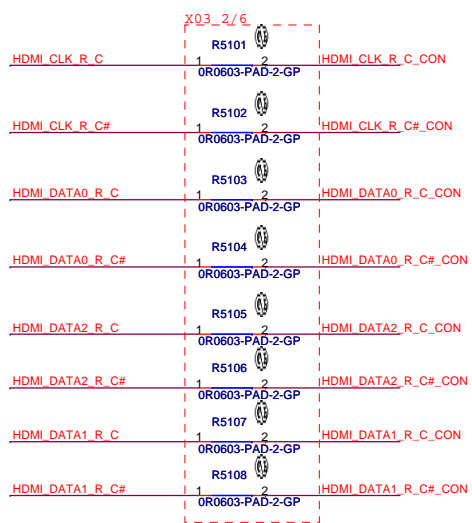
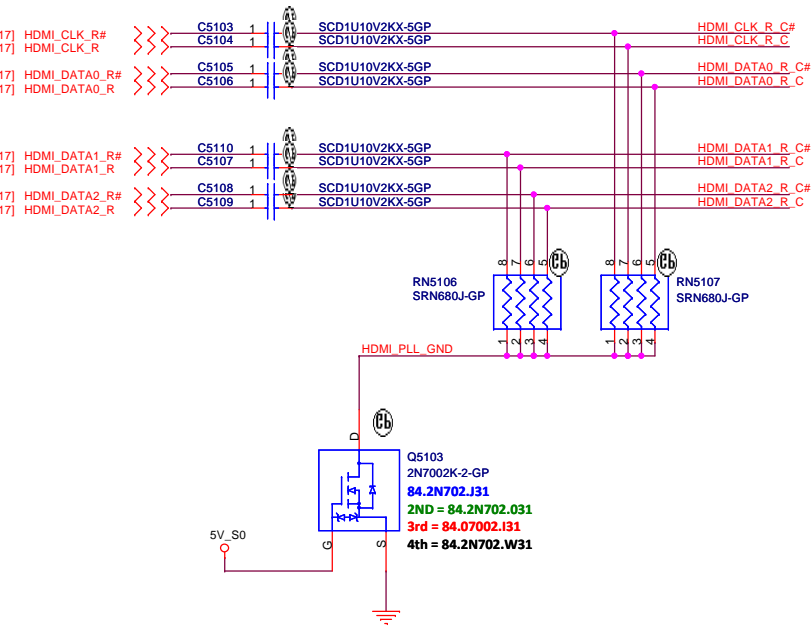
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HDMI Level Shifter



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Title: **HDMI Level Shifter/Connector**

Size A3 Document Number: **BMW Z4 DIS** Rev **A00**

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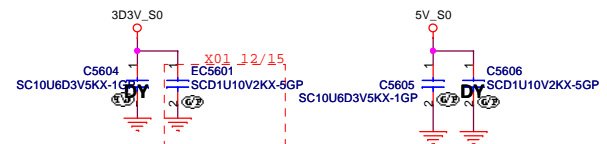


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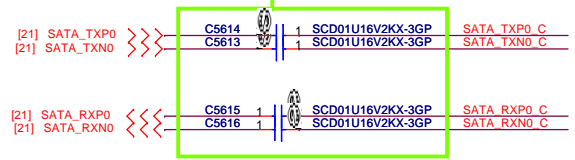
ITP/Fan Connector

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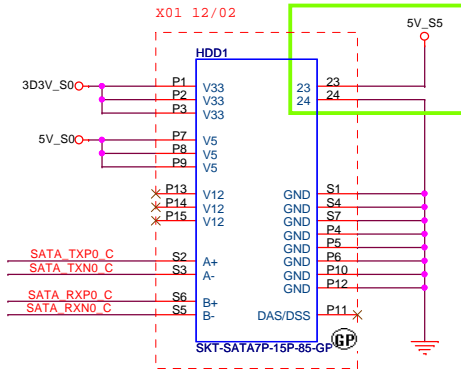


Layout Note:

AC coupling Cap:
place near CONN(<100mils)



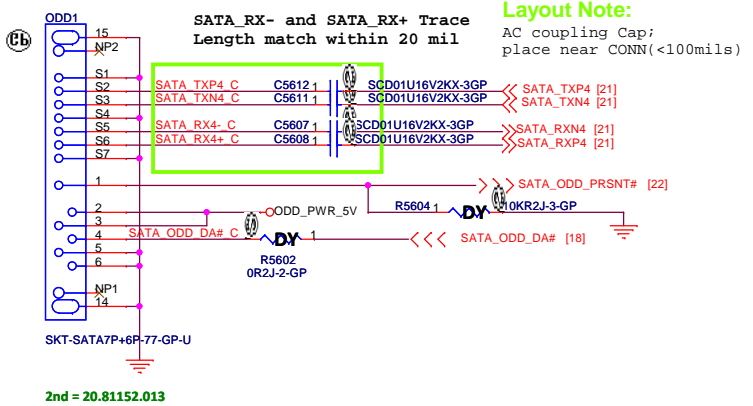
HDD CONN



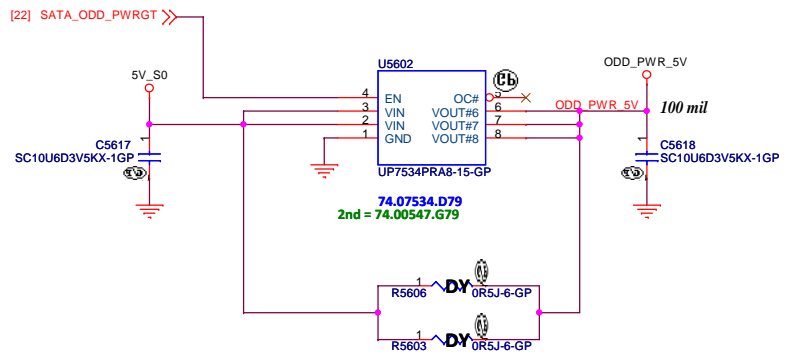
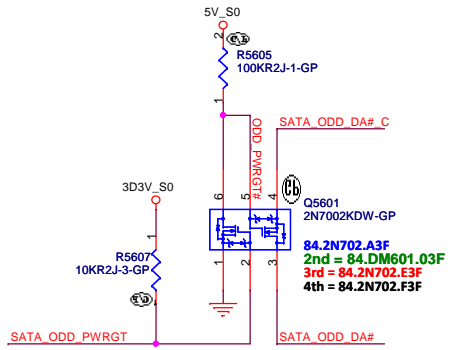
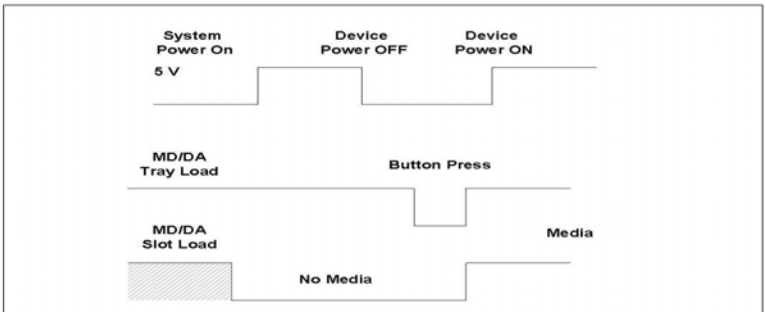
Due to layout, HDD1 pin 23 modify 5V_S5

20.81599.022
2nd = 22.10300.C51

ODD CONN



Zero Power ODD Power Sequence



<Core Design>

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Title					
HDD/ODD					
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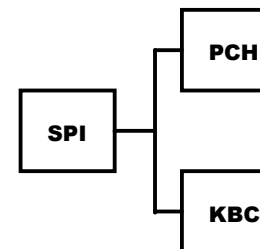
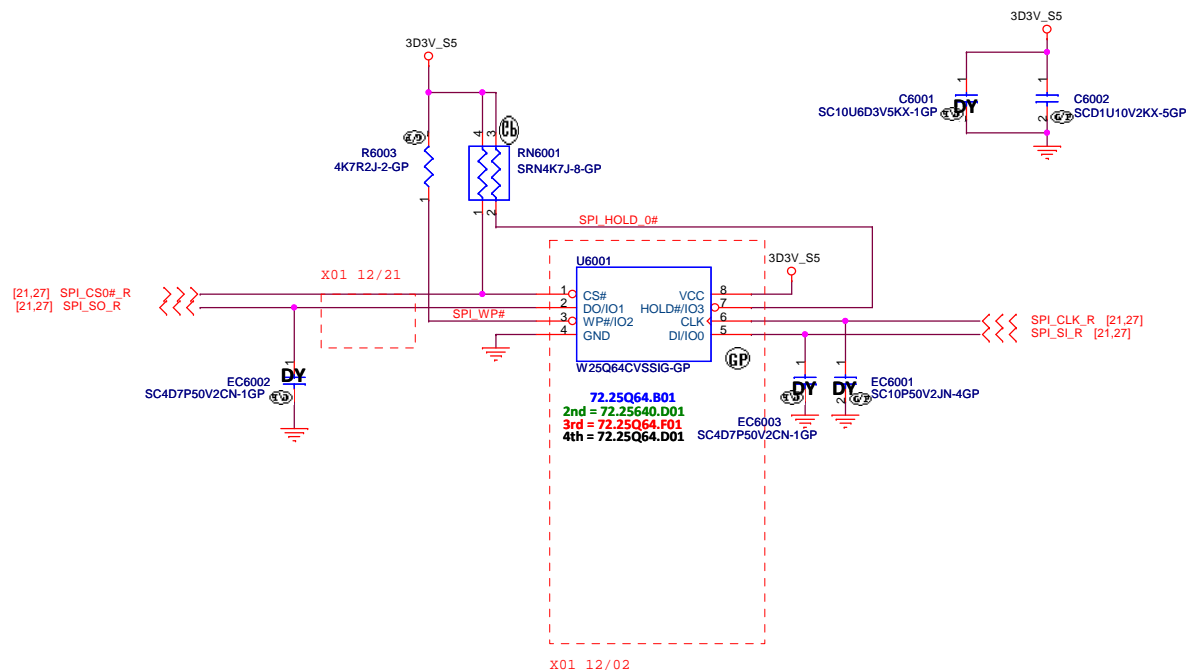
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SSID = Flash.ROM

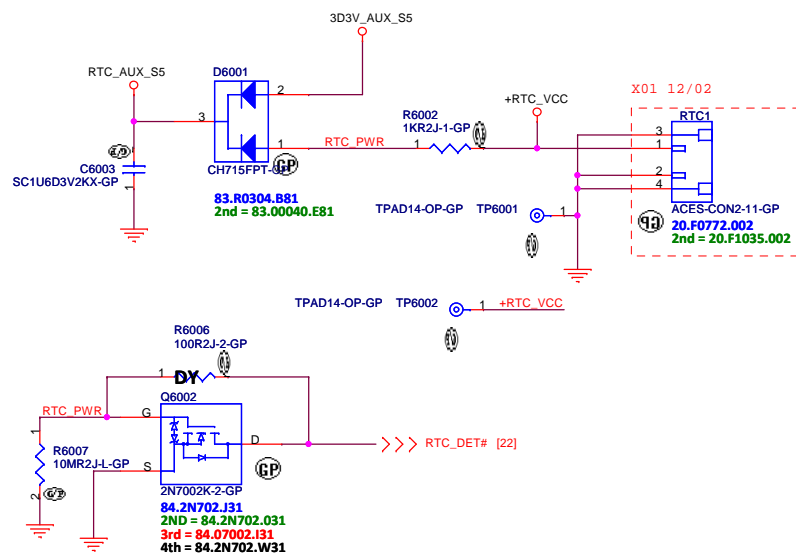
SPI Flash ROM(8M) for PCH



Layout Note:

KBC---10"---PCH
KBC---1.5"~6.5"---SPI
PCH---0.5"~6.5"---SPI

SSID = RBATT



<Core Design>




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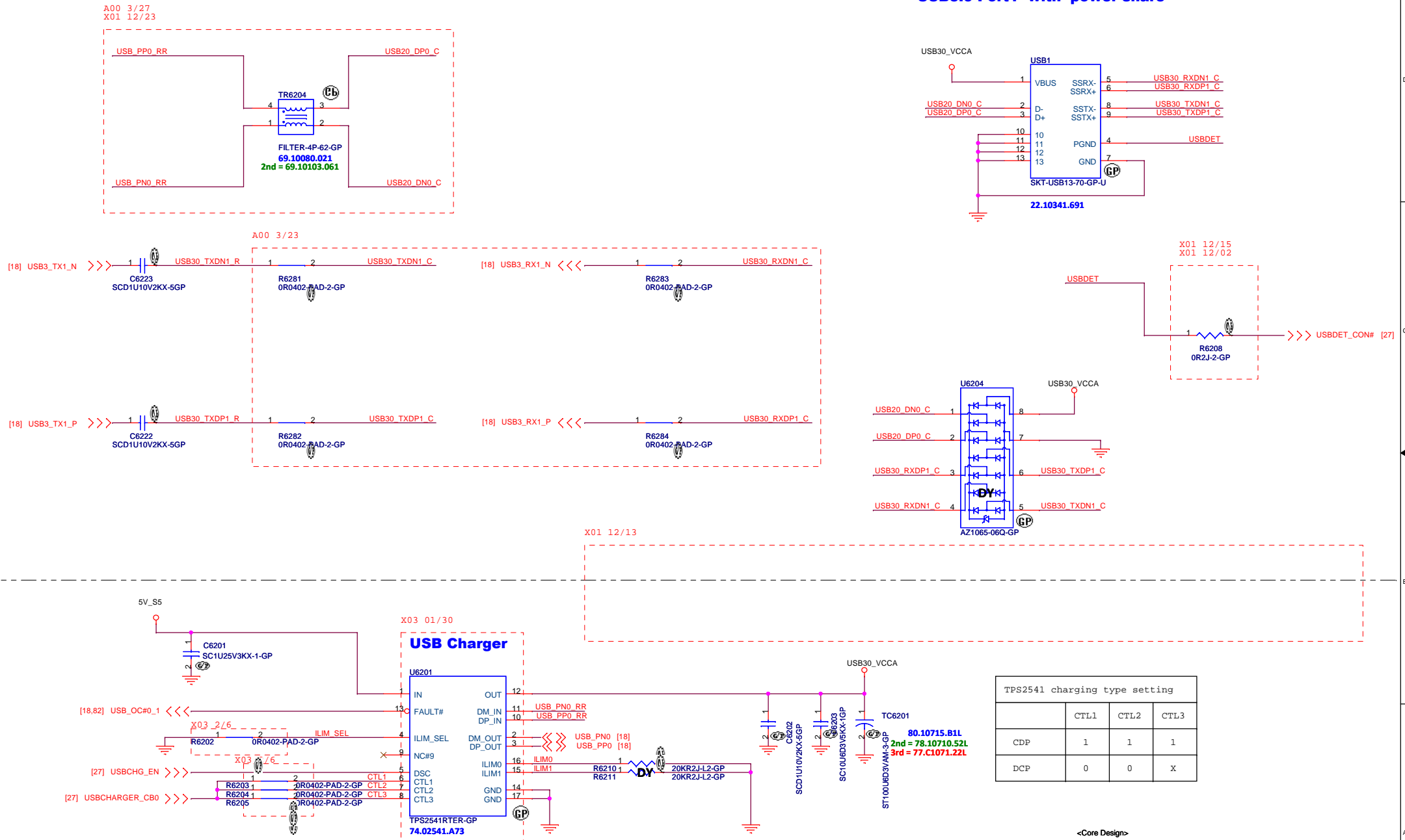
BMW Z4 DIS

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USB3.0 Port1 with power share



TPS2541 charging type setting			
	CTL1	CTL2	CTL3
CDP	1	1	1
DCP	0	0	X

<Core Design>

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USB 3.0

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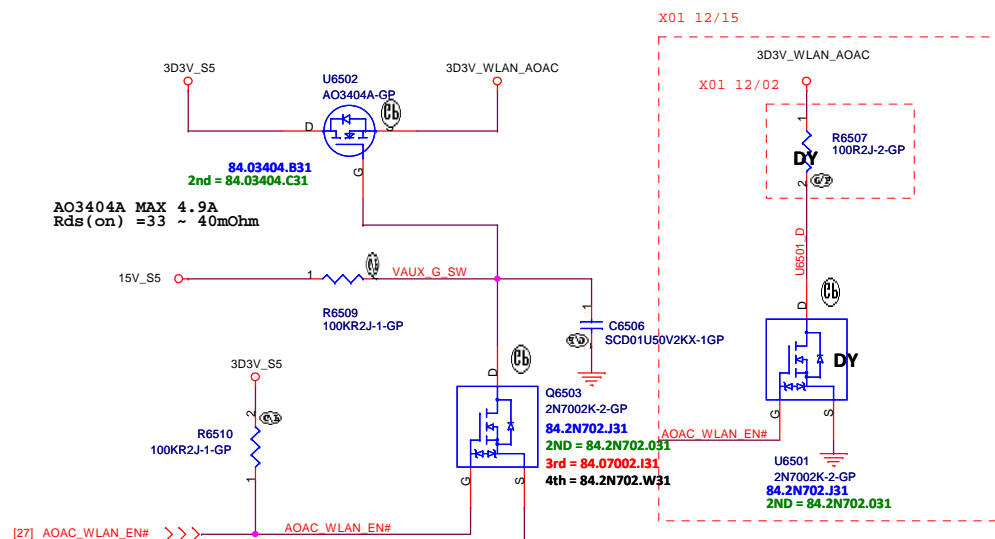
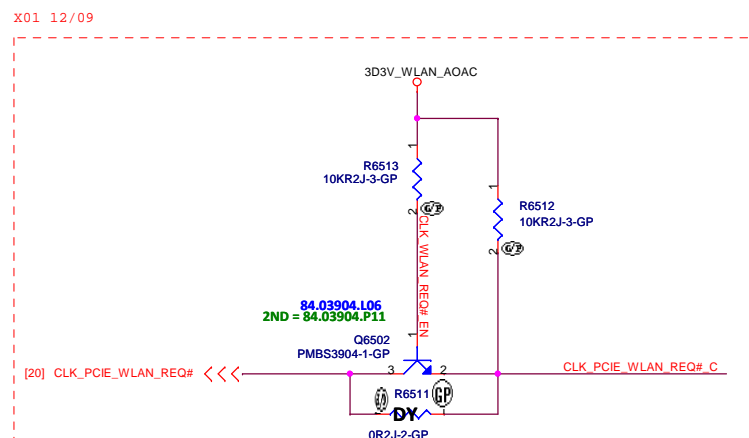
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Finger Printer		
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WLAN/BT

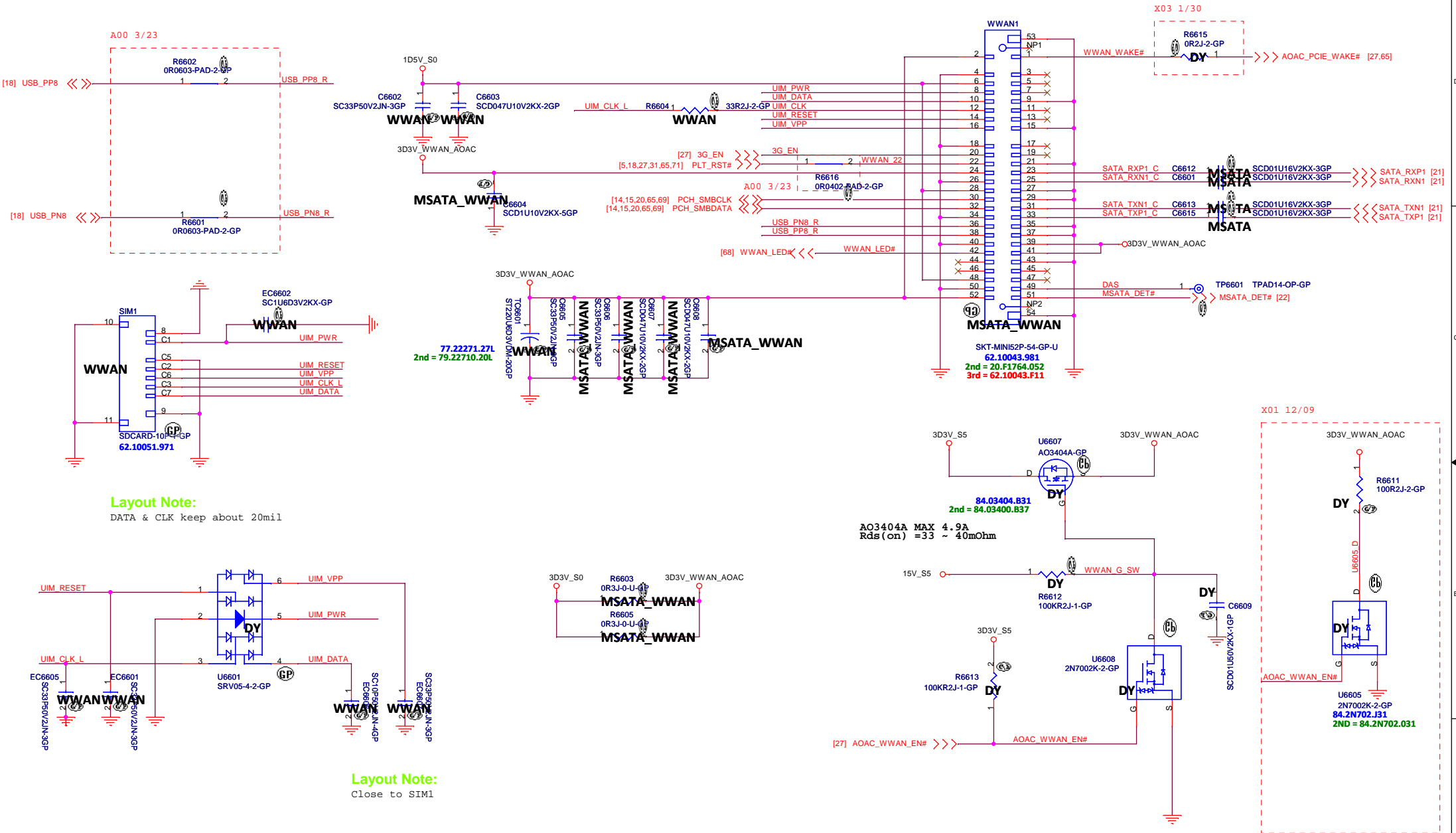
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WWAN CONN



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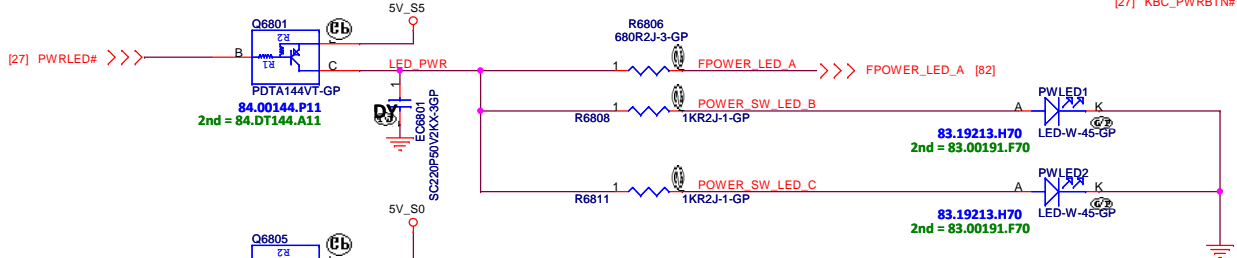
Document Number
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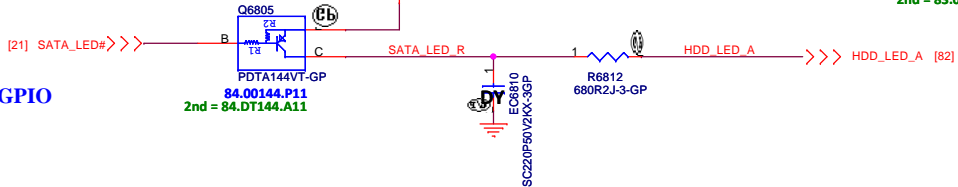
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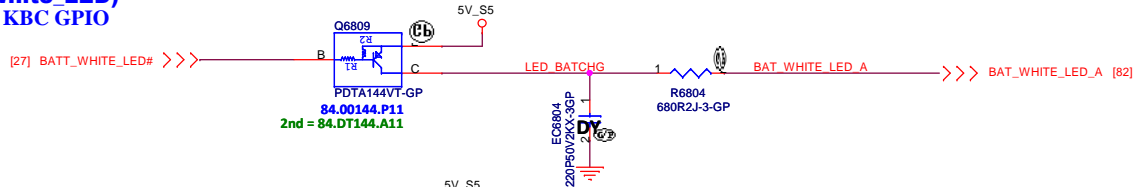
Front Power LED
LOW acted from KBC GPIO



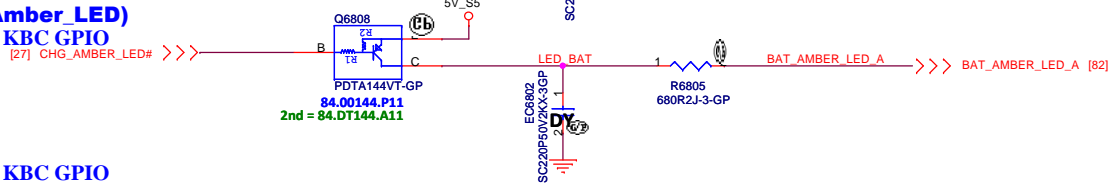
SATA HDD LED
LOW acted from PCH GPIO



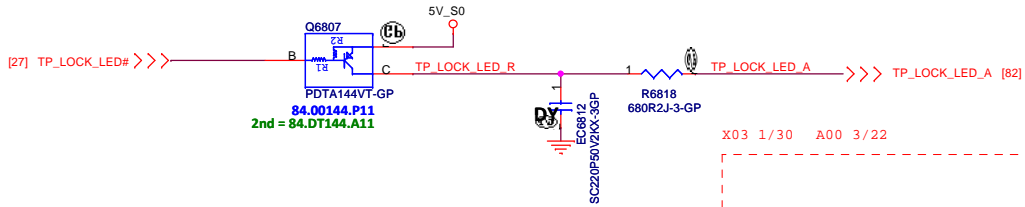
Battery LED2(White_LED)
LOW acted from KBC GPIO



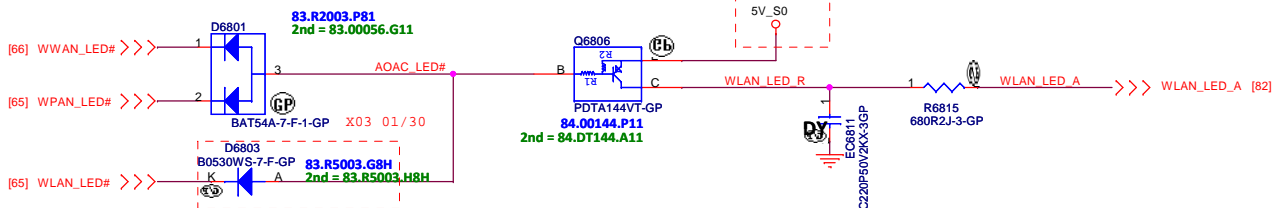
Battery LED1(Amber_LED)
LOW acted from KBC GPIO



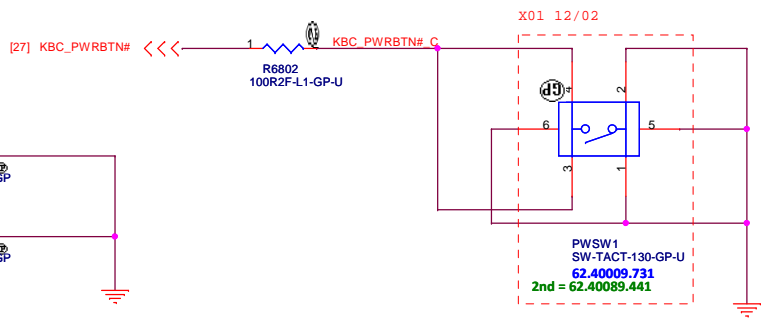
TPLOCK LED
LOW acted from KBC GPIO



WLAN LED
LOW acted from KBC GPIO

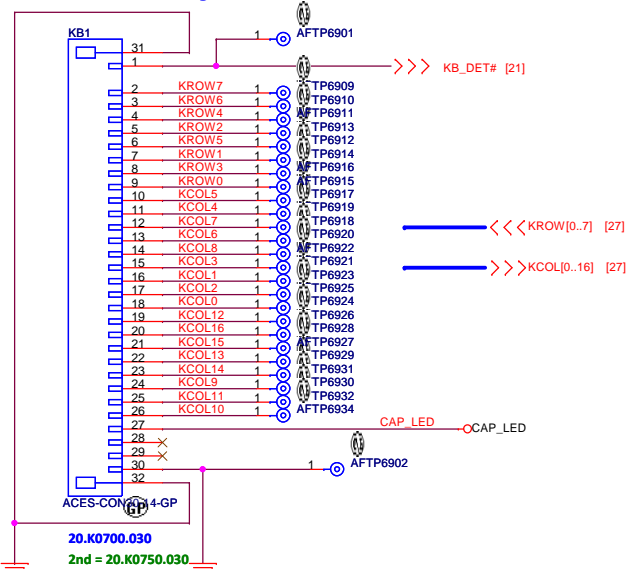


PWRBTN

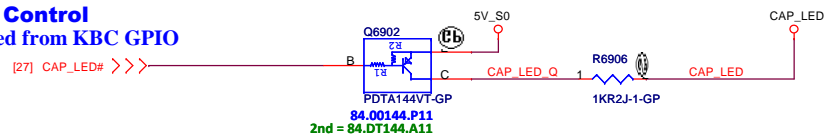


SSID = KBC

Internal Keyboard Connector

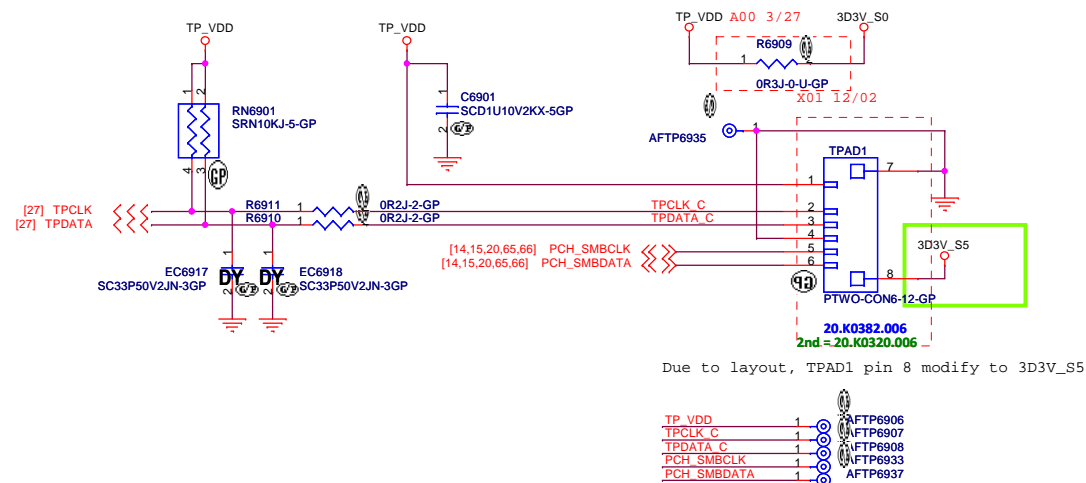


CAP LED Control LOW acted from KBC GPIO



SSID = Touch.Pad

Touch Pad Connector



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Key Board/Touch Pad

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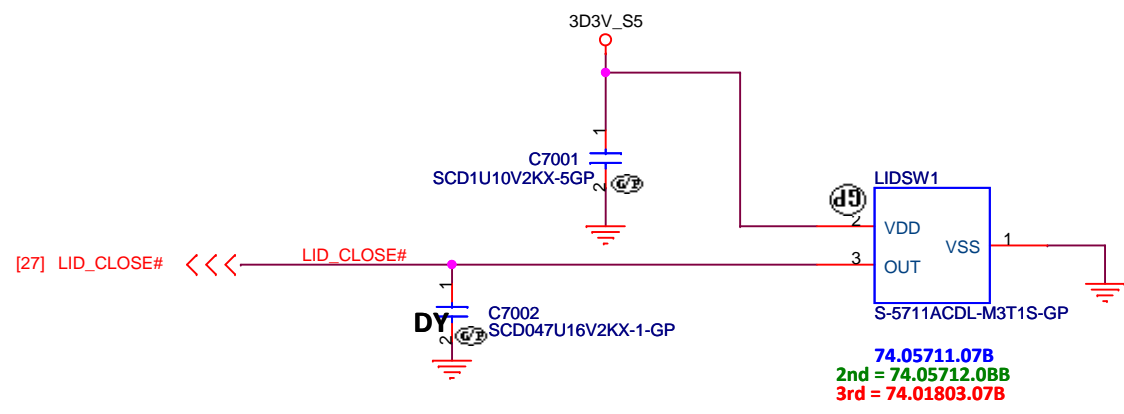
A00

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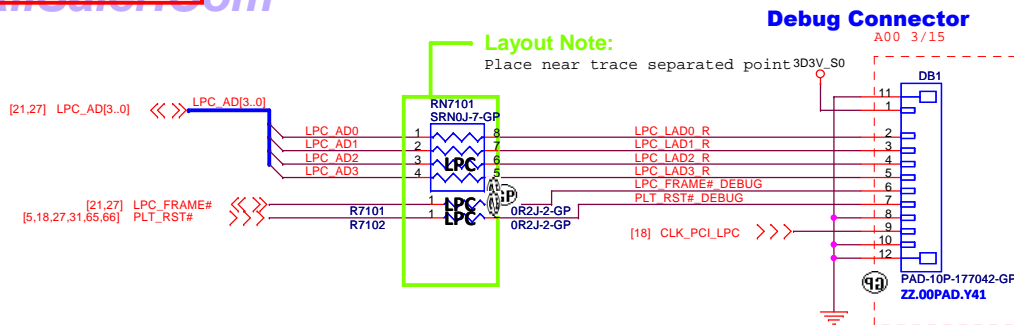
SSID = User.Interface



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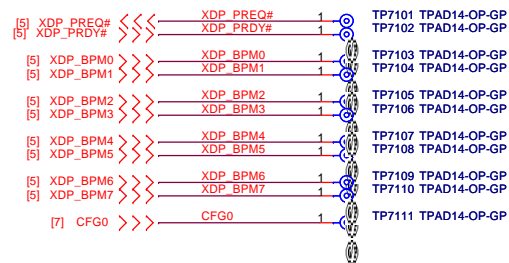
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Hall Sensor			
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SSID = DEBUG PORT



SSID = CPU

CPU XDP



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Title Dubug connector			
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Title

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Size
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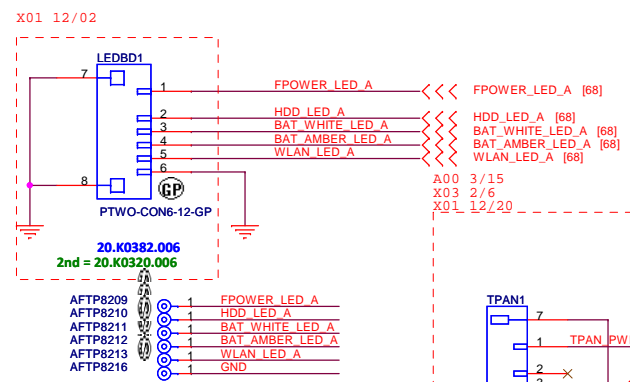
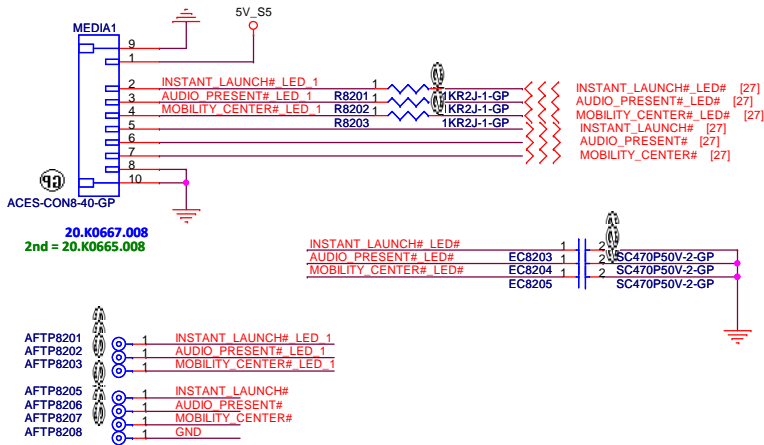
Document Number
BMW Z4 DIS

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A00

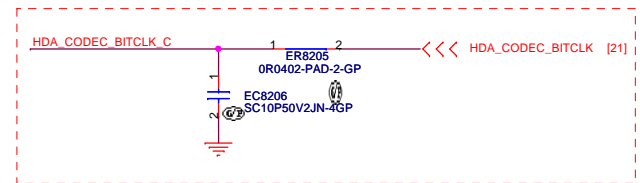
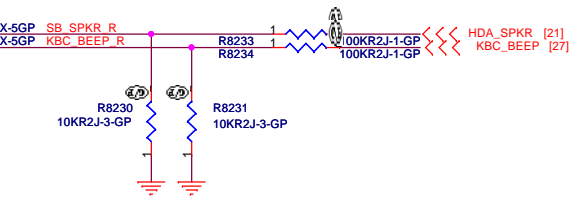
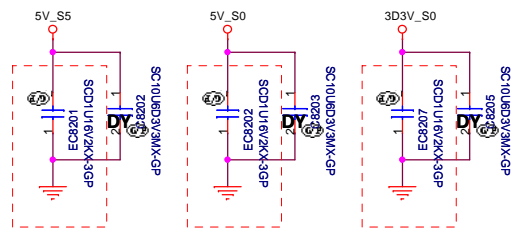
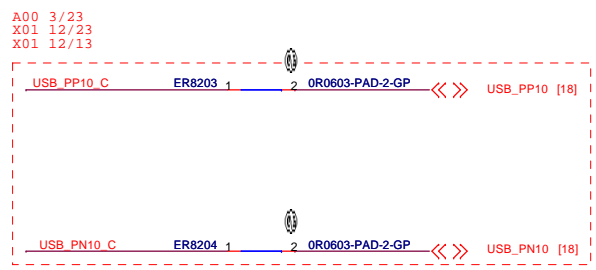
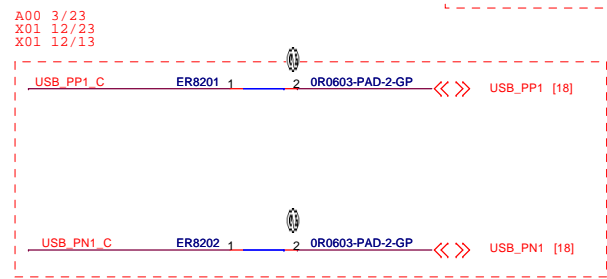
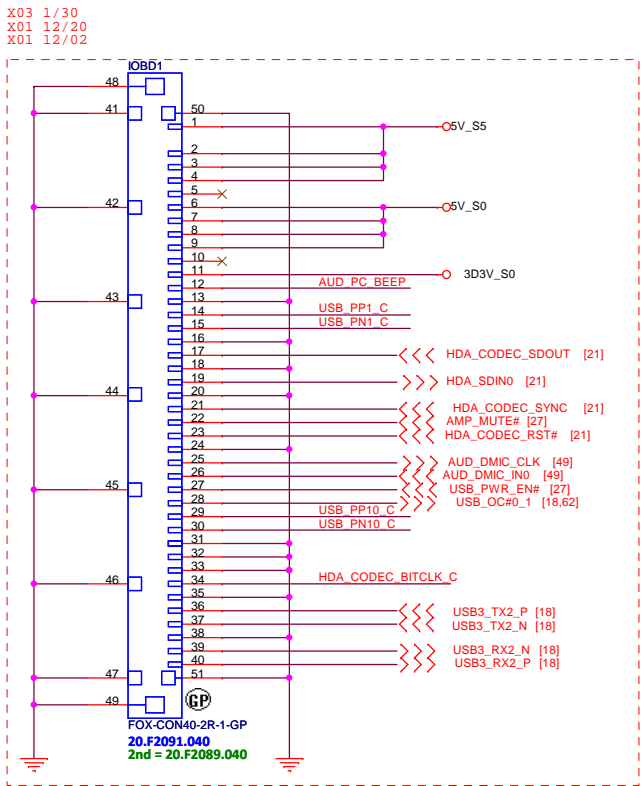
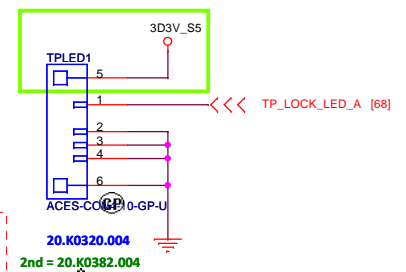
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SSID = User Interface



Due to layout, TPLED1 pin 5 modify 3D3V_S5



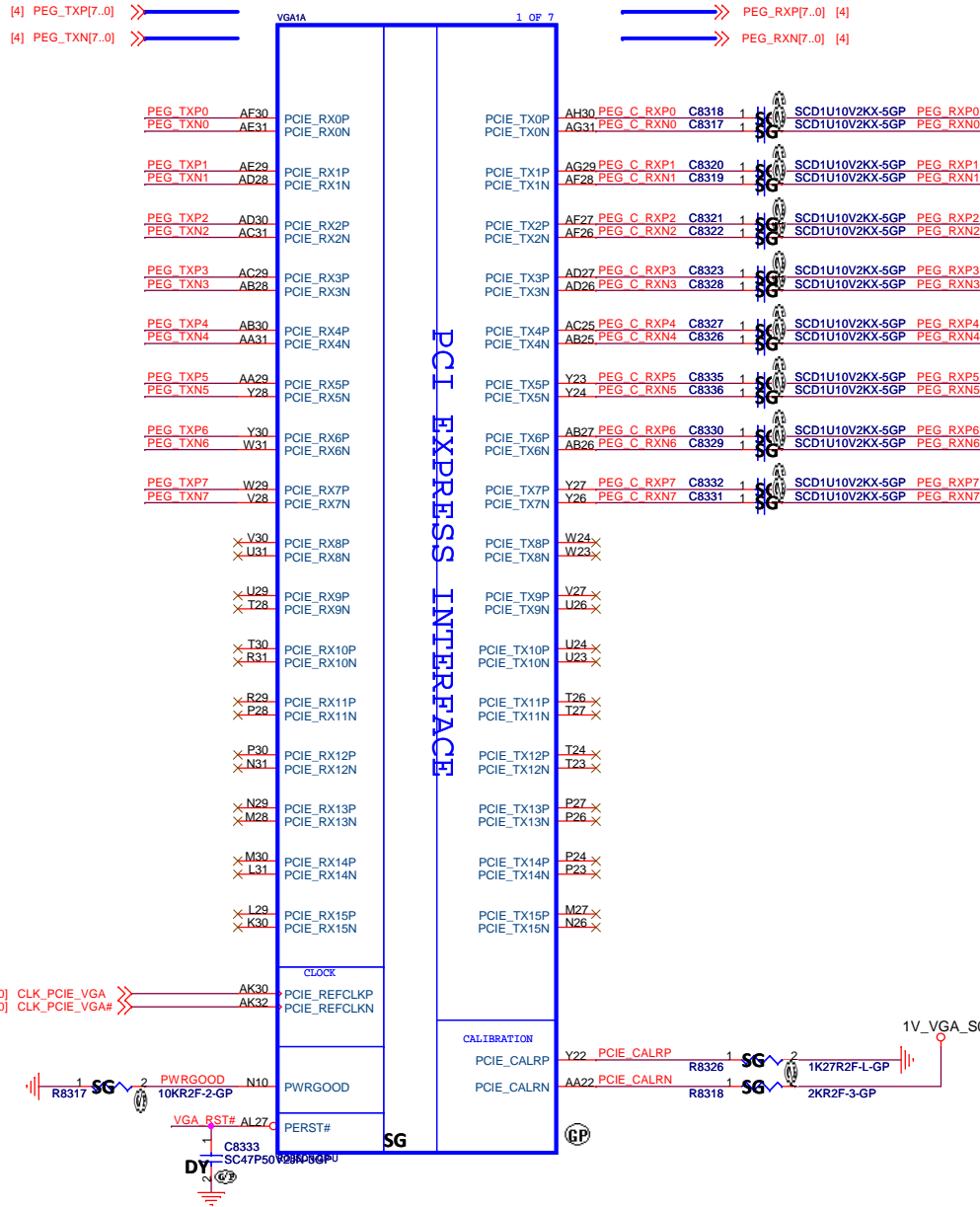
<Core Design>

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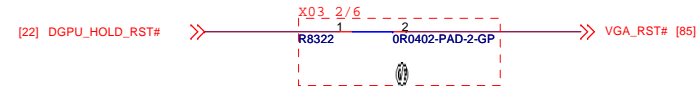
Title: **IO Board Connector**

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X01 12/15

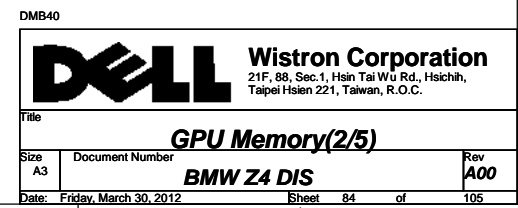


<Core Design>



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Title		GPU PEG/STRAPPING(1/5)	
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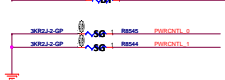
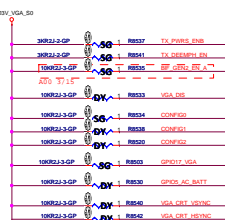


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED	PLATFORM
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCIe device as 2.50 Gb/s capable at power on 1: Advertises the PCIe device as 5.00 Gb/s capable at power on	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low	?	0
GPIO8_ROMSO	GPIO8	0: VGA Controller capacity enabled 1: The device won't be recognized as the system's VGA controller	0	0
VGA_DIS	GPIO9	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	0	0
ROMIDCFG2_0	GPIO[13:11]	BIOS ROM ID Config[2:0] defines the ROM type BIOS_ROM_0=0, BIOS_ROM_1=1, BIOS_ROM_2=2	X X X	0 0 1 (2 0 0 0 1)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO22_ROMCEN	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	X	0
VP_DEVICE_STRAP_IN	VZSYNC	VP Device Strap Indecider to be software driver that it sense whether or not a VP device is connected on the VP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

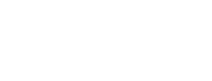
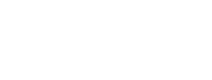
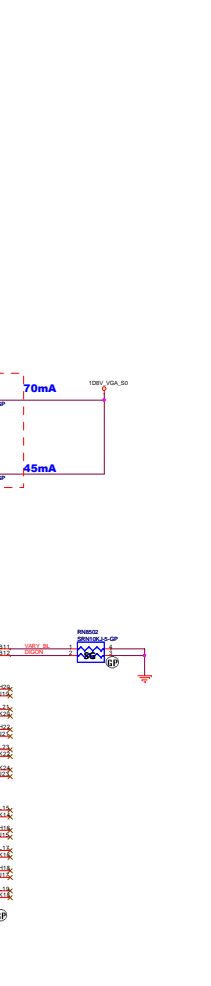
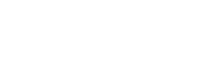
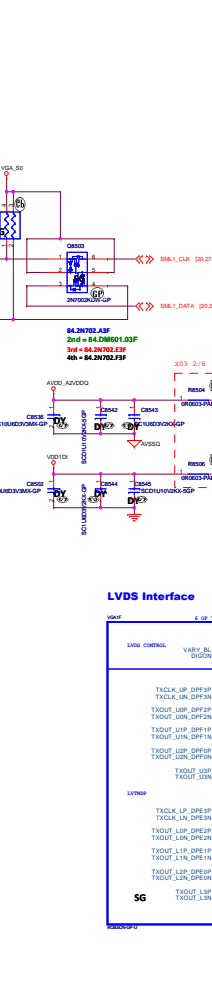
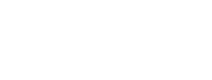
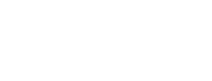
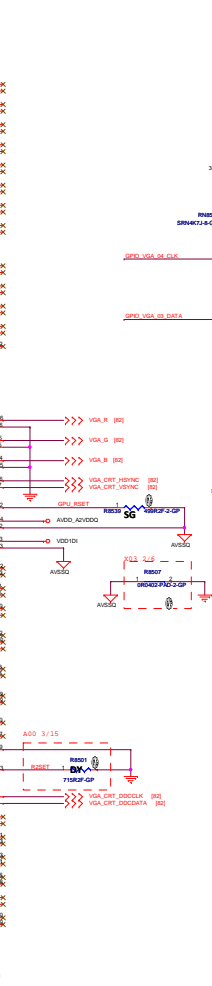
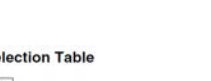
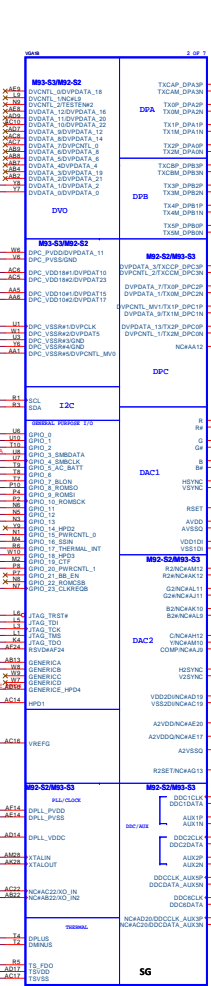
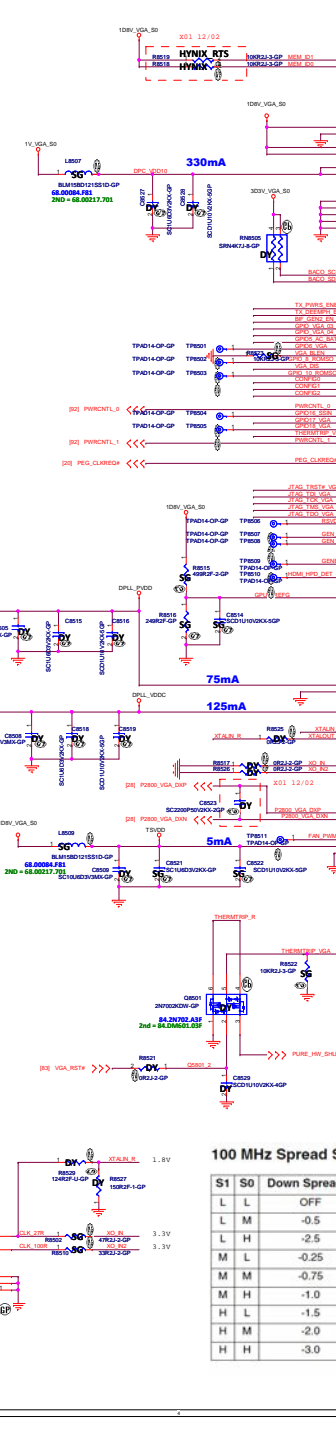
Straps Pin



MEMORY ID Table

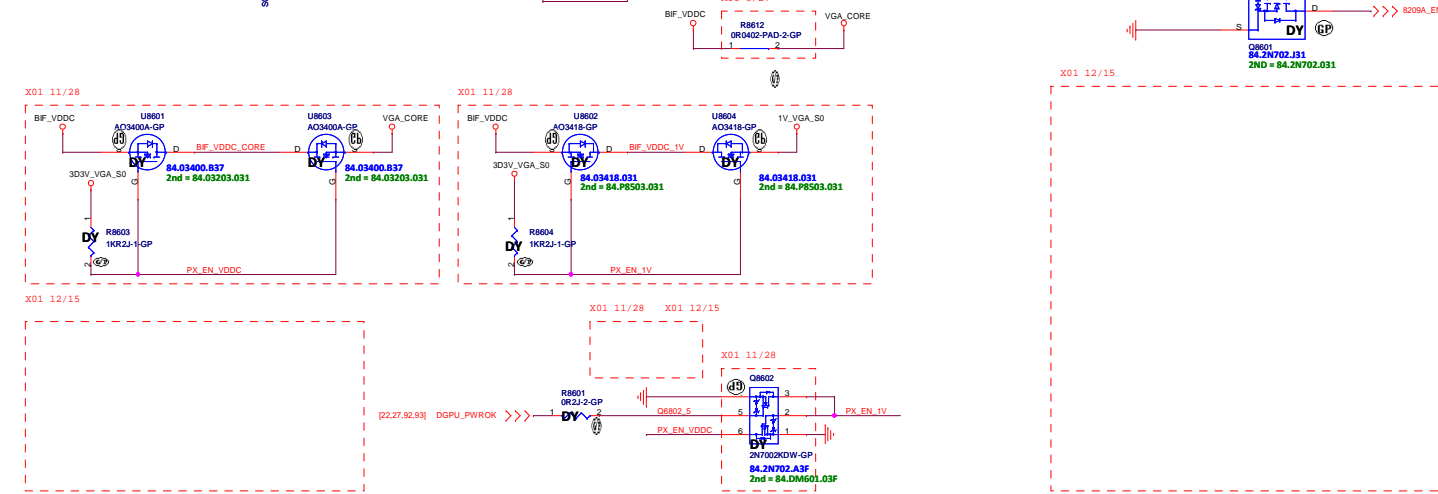
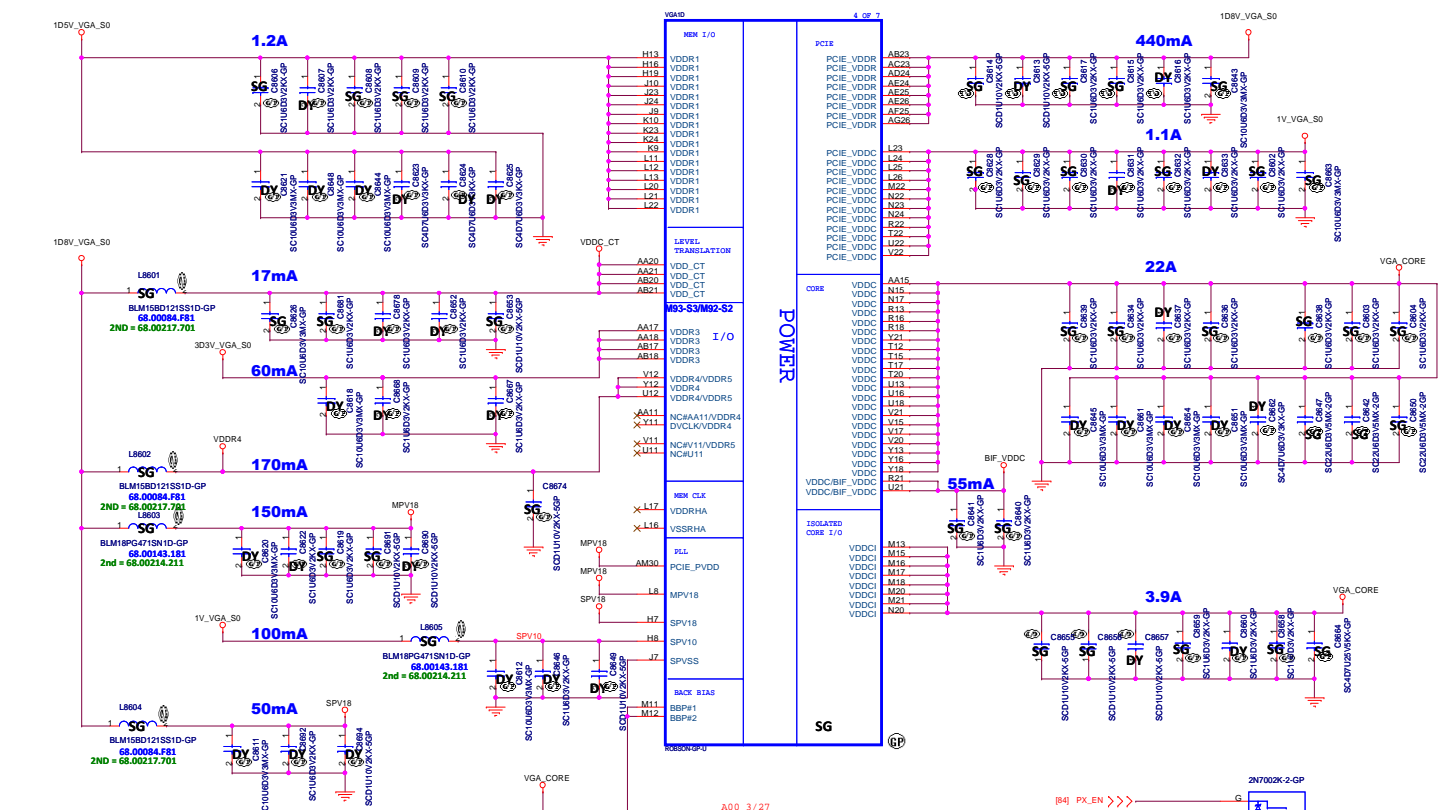
DVPPDATA[3:0]	Description
0011	GD0R5 1.250GHz Rynlx-H5Q2H24MFR-T2C 128M*16
0001	GD0R5 1.250GHz Rynlx-H5Q2H24MFR-T2C 128M*16
0000	GD0R5 1.250GHz SAM000H-R4G20325FD-PC04 128M*16

DVPPDATA[0:3] Default: Pull down



100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0



Mode	PX_EN	PX_EN_1V	PX_EN_VDDC	BIF_VDDC
DIS	Low	Low	High	VGA_CORE
BACO	High	High	Low	1V_VGA_S0

POP	Q8601, Q8602, R8601, U8601, U8602, U8603 U8604, R8603, R8604, R8408
DY	R8612

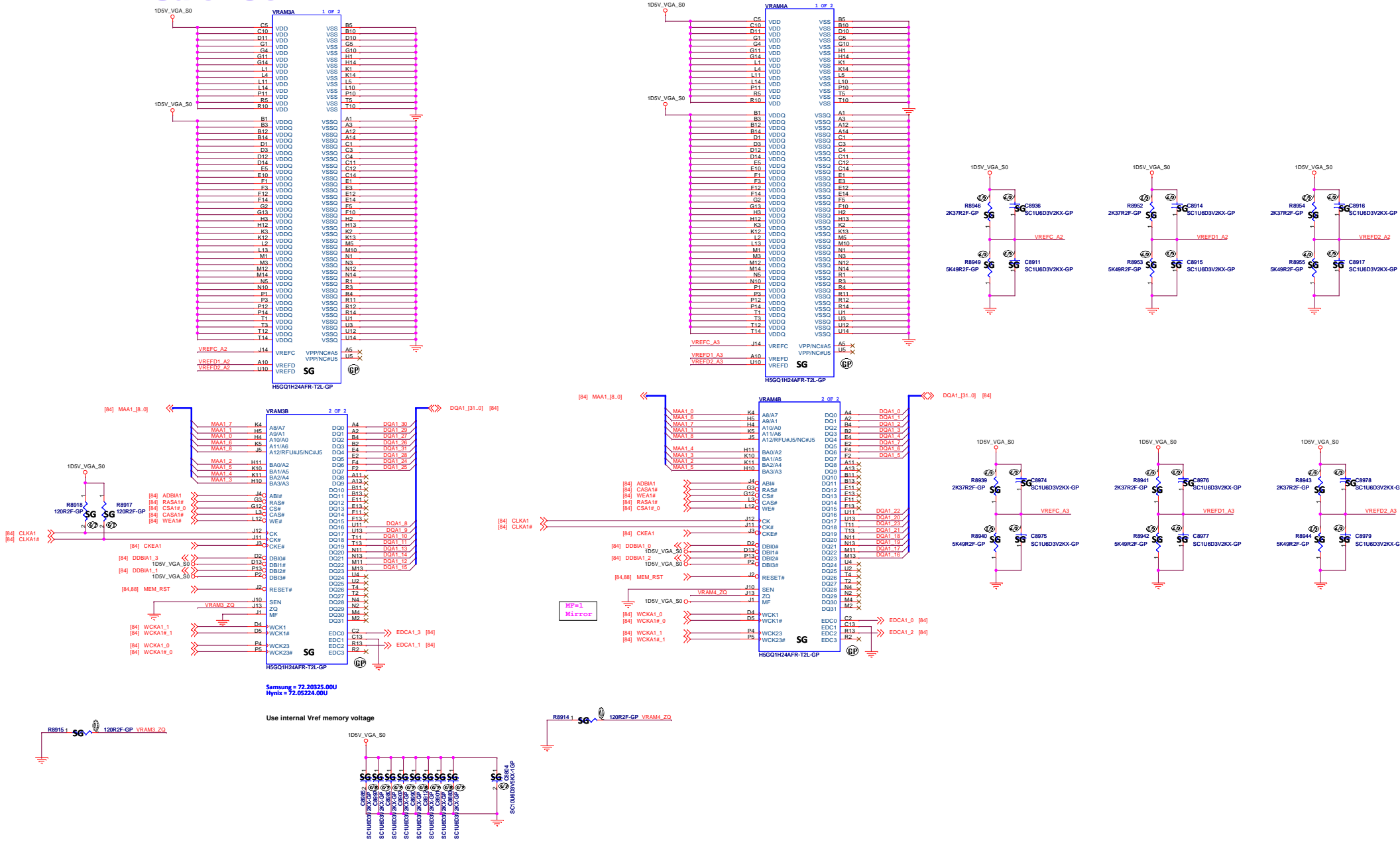
POP	R8612
DY	Q8601, Q8602, R8601, U8601, U8602, U8603 U8604, R8603, R8604, R8605, R8408

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**GPU_DPPWR/GND(5/5)**Rev
400


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Title

Reserved

Size
A3

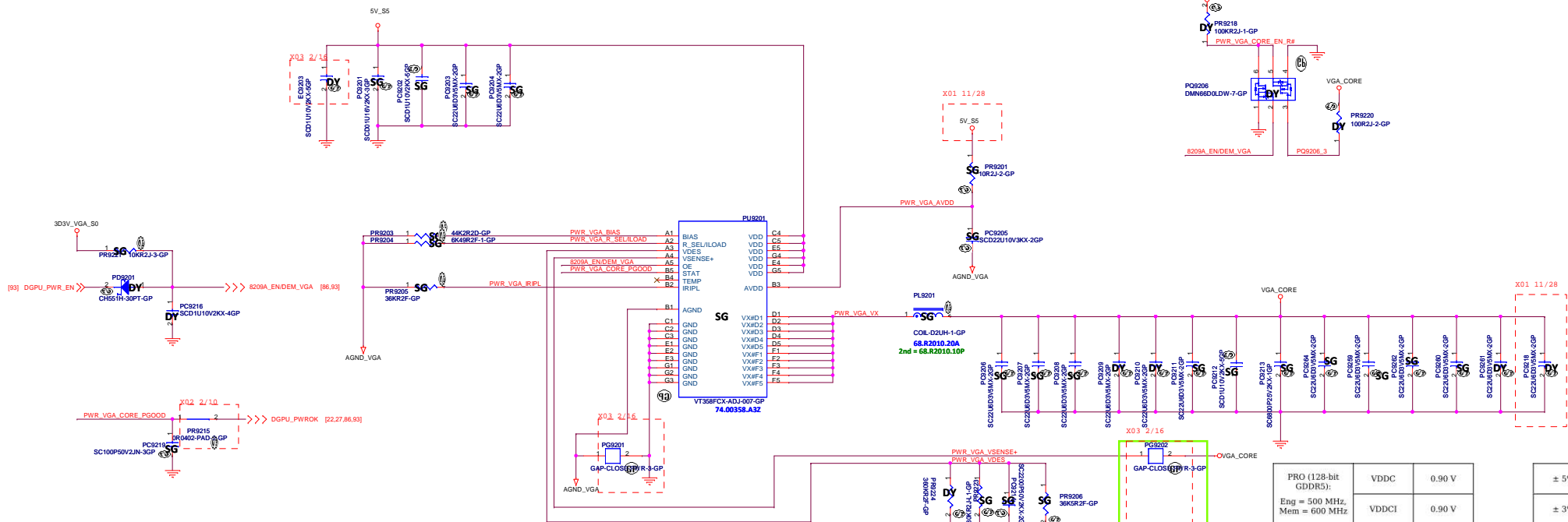
Document Number
BMW Z4 DIS

Rev
A00

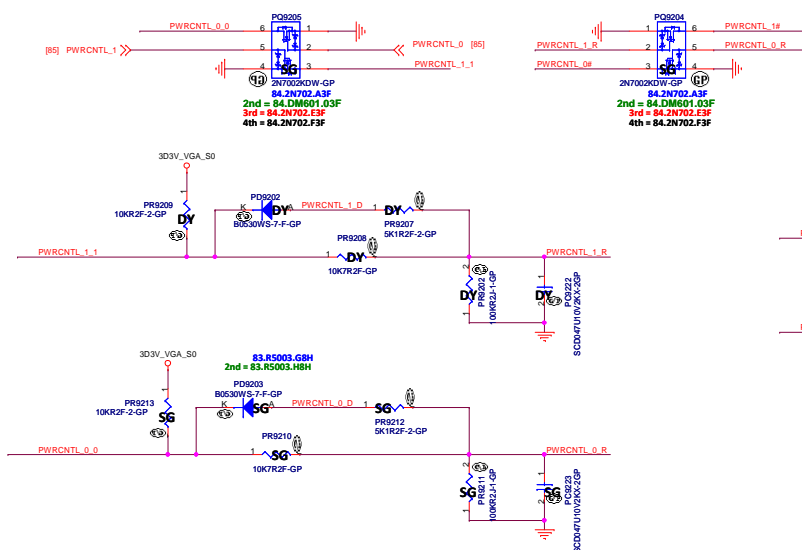
Date: Friday, March 30, 2012

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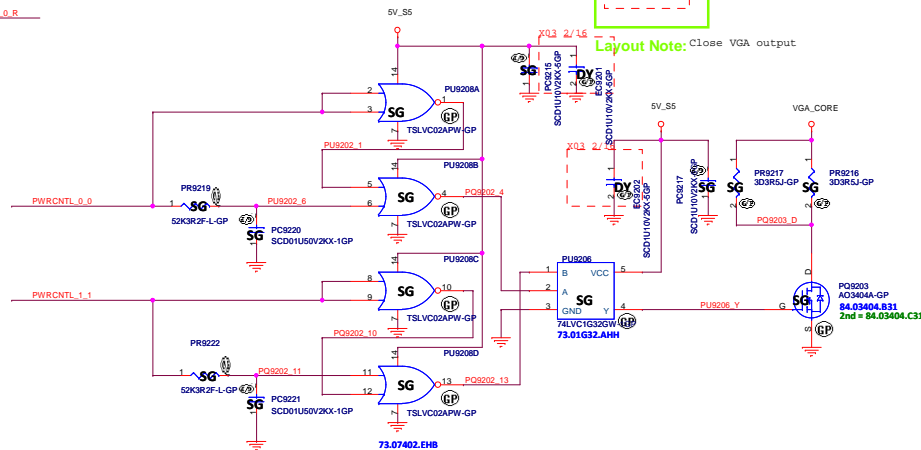
```
SSID = PWR.Plane.Regulator_vga_core
```



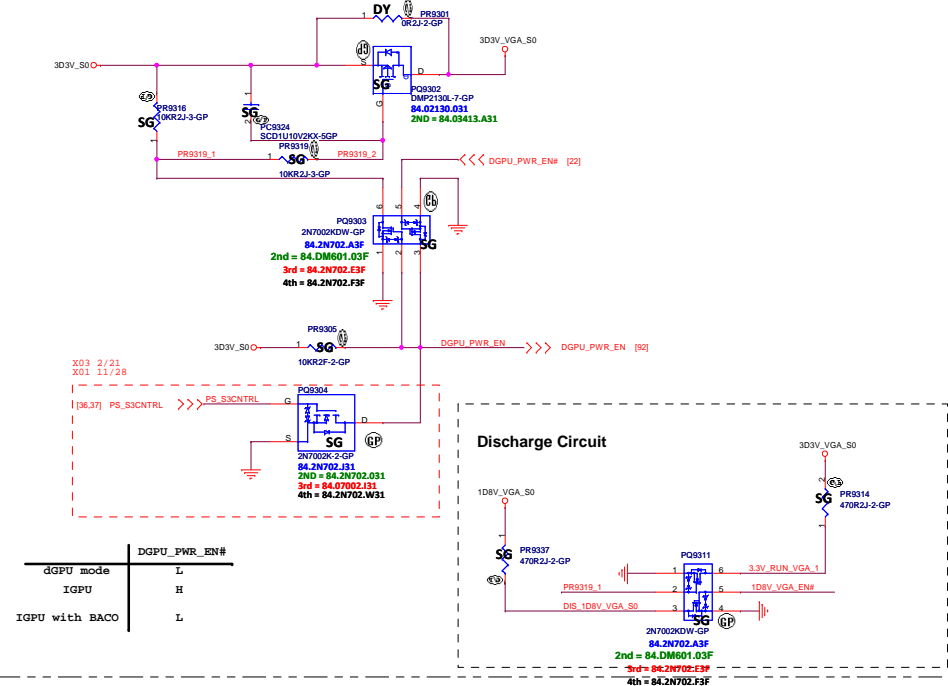
PRO (128-bit GDDR5): Eng = 500 MHz, Mem = 600 MHz	VDDC	0.90 V	± 5%	16.0 A (RMS) 22.0 A (Peak)
	VDDCI	0.90 V	± 3%	3.3 A (RMS) 3.9 A (Peak)



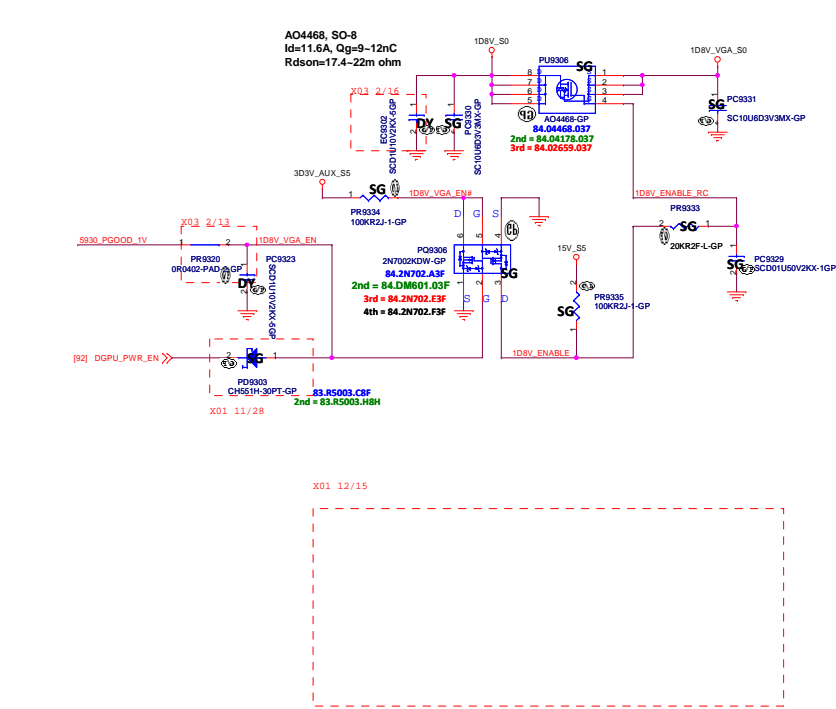
VID0 GPIO15	Voltage
1	1V
0	0.9V



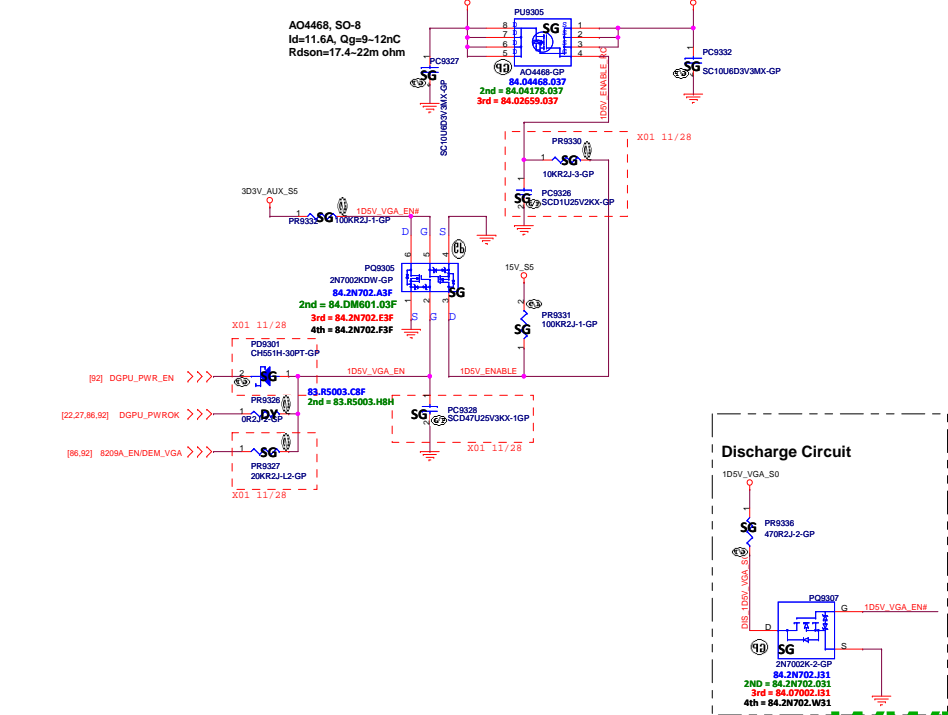
3D3V_S0 to 3D3V_VGA_S0 Transfer



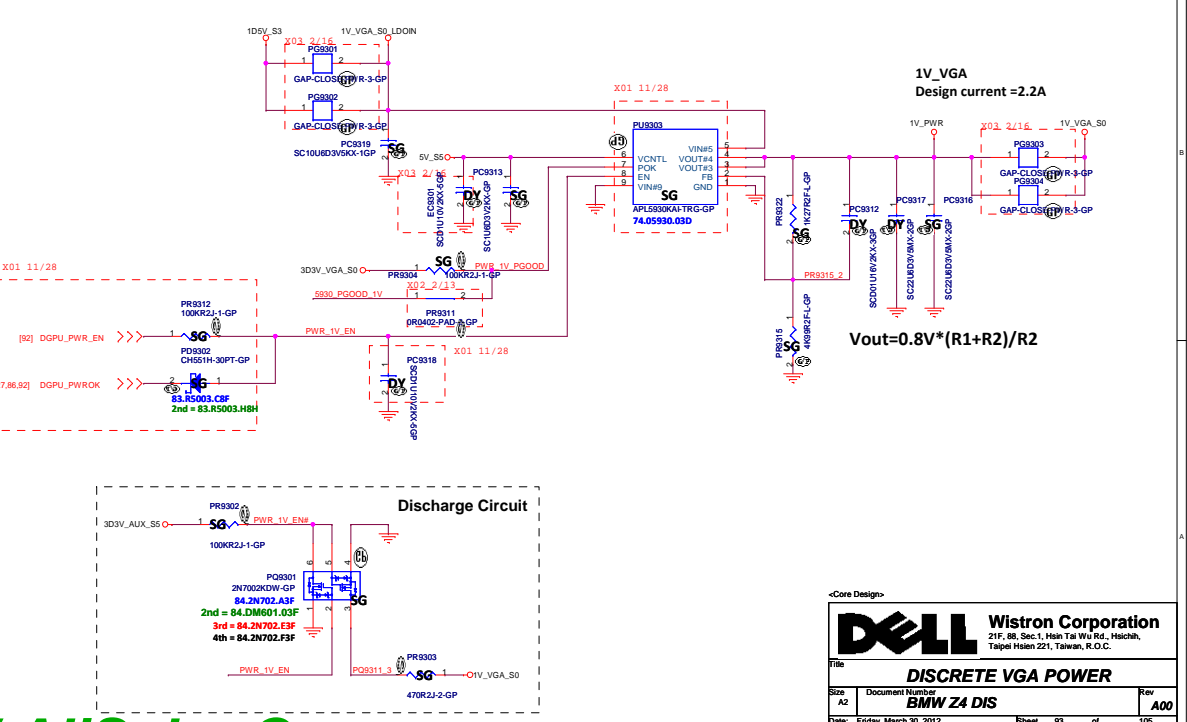
1D8V_S0 to 1D8V_VGA_S0 Transfer



1D5V_S3 to 1D5V_VGA_S0 Transfer




APL5930 for 1V_VGA_S0



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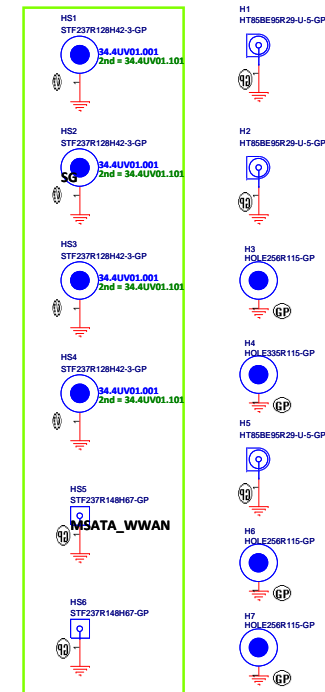
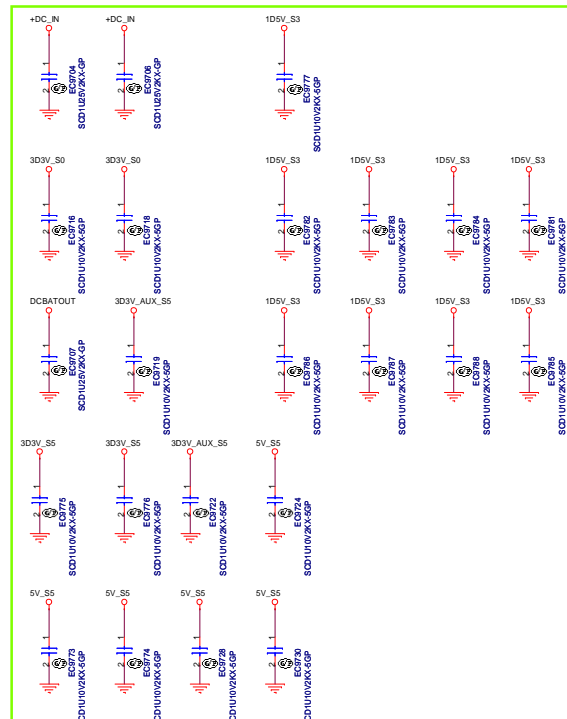
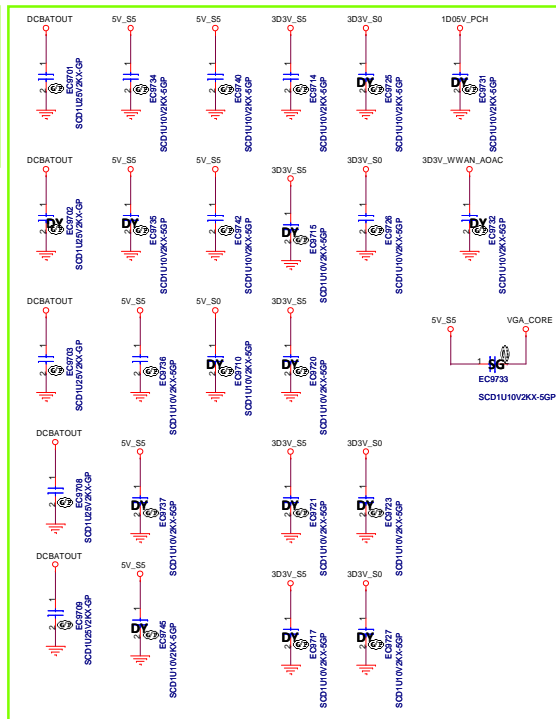
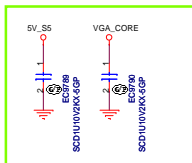
Date: Friday, March 30, 2012

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Reserved

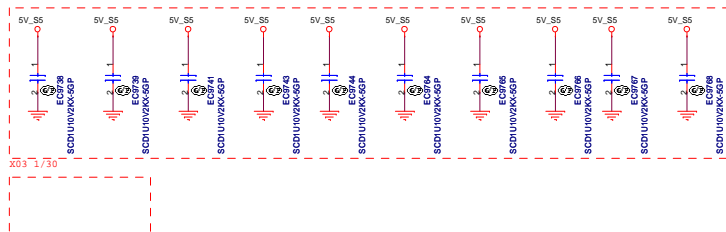
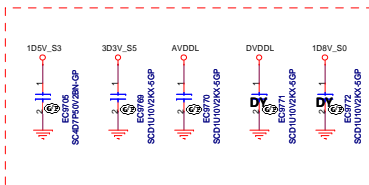
RF

EMI x



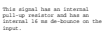
X01 12/15 For RF

X01 12/09 For EMI X01 12/30

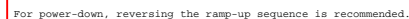


X01 12/2

red word: KBC GPIO



Thames PRO Power-Up/Down Sequence



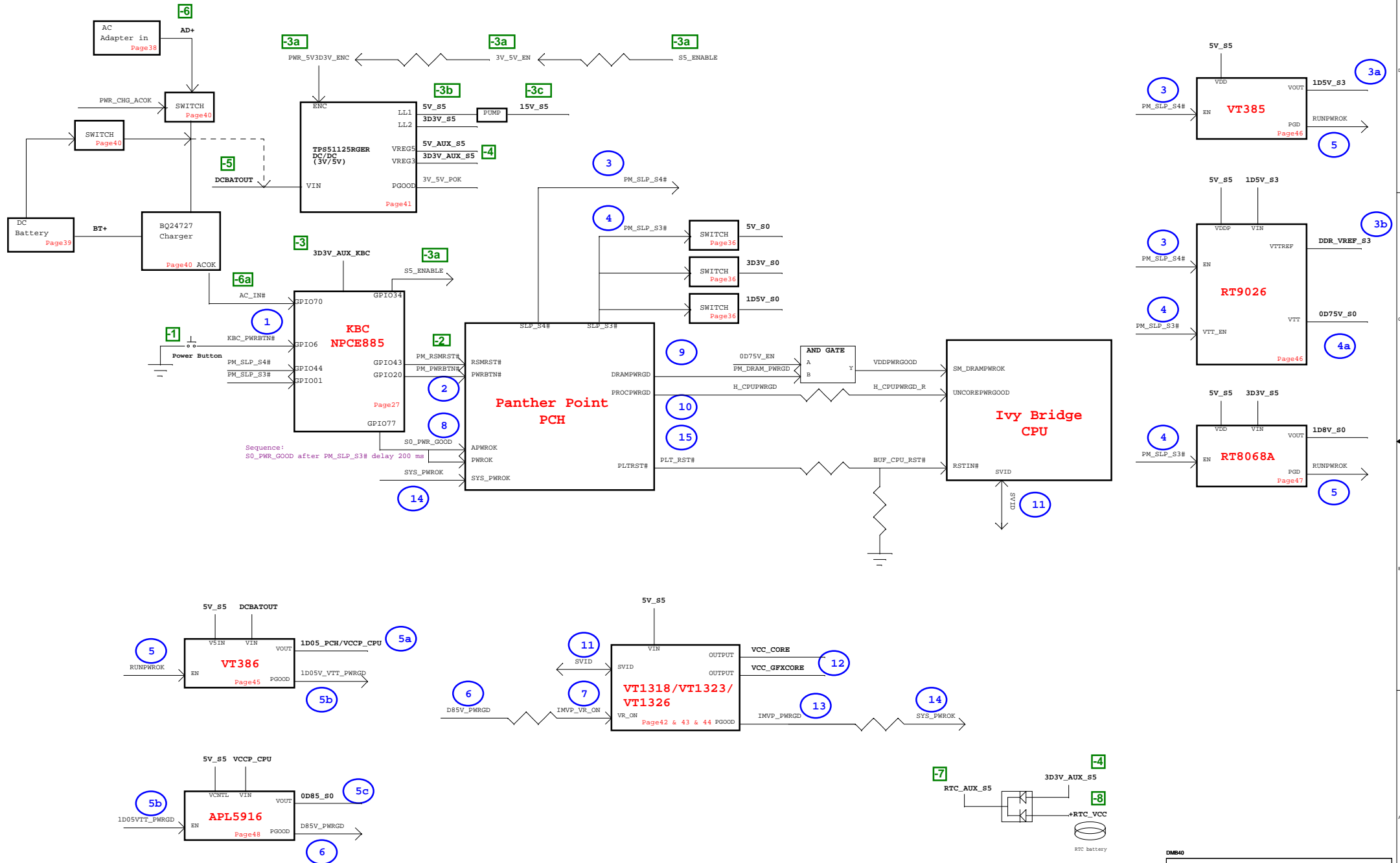
red word: KBC GPIO



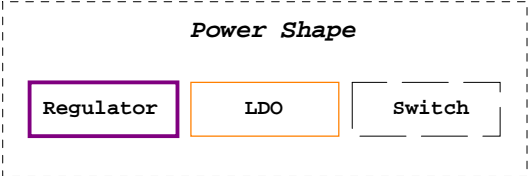
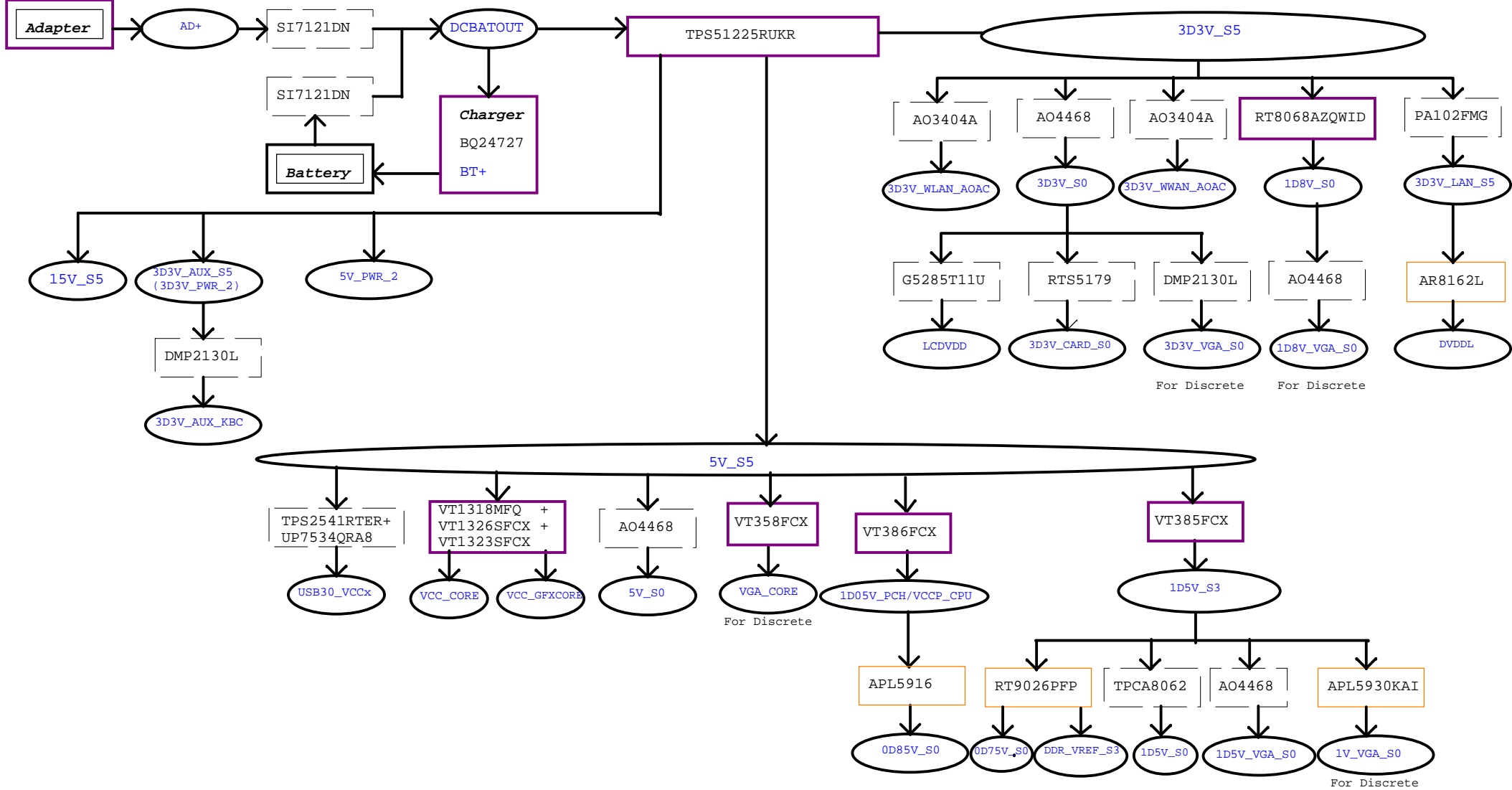
VREF_Sus must be powered up before VocSus1_3, or after VocSus1_3 within 0.7 V. Also, VREF_Sus must power down after VocSus1_3, or before VocSus1_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

Wistron CHIEF RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 15



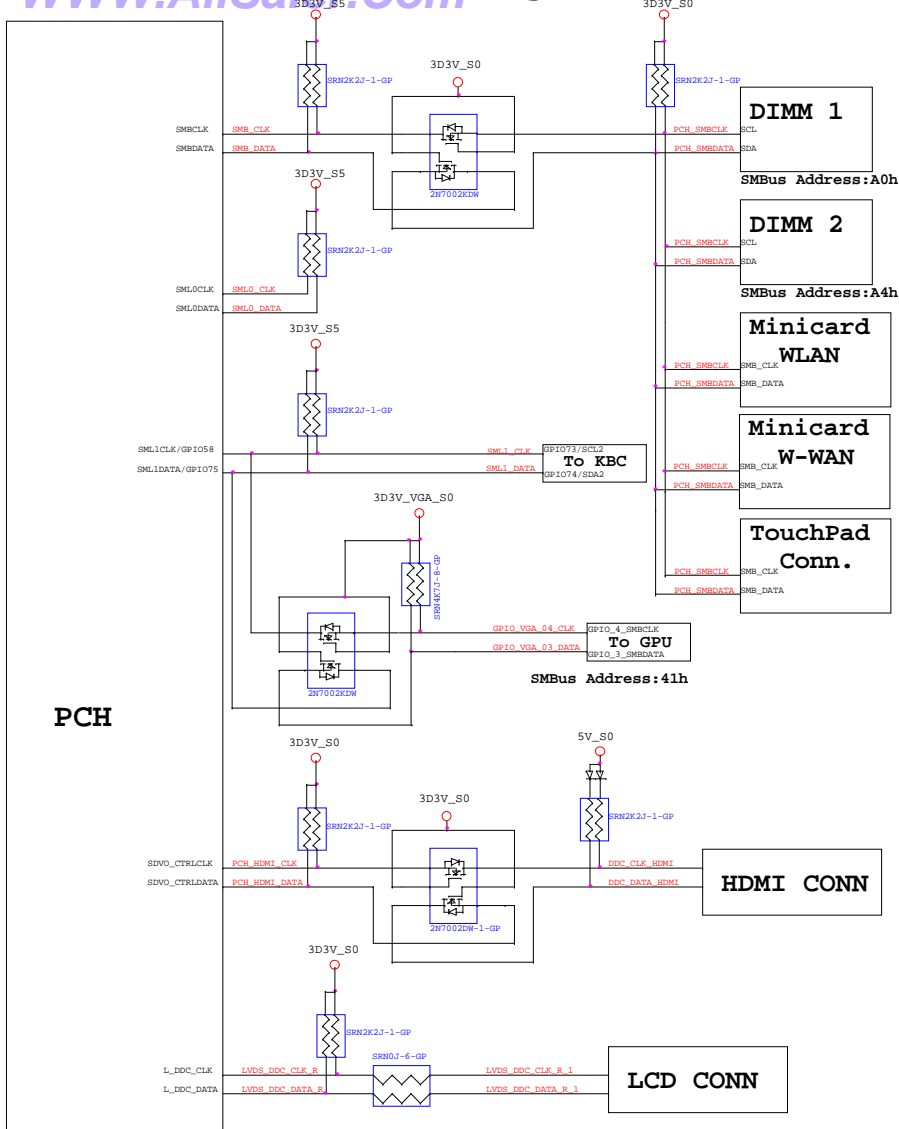
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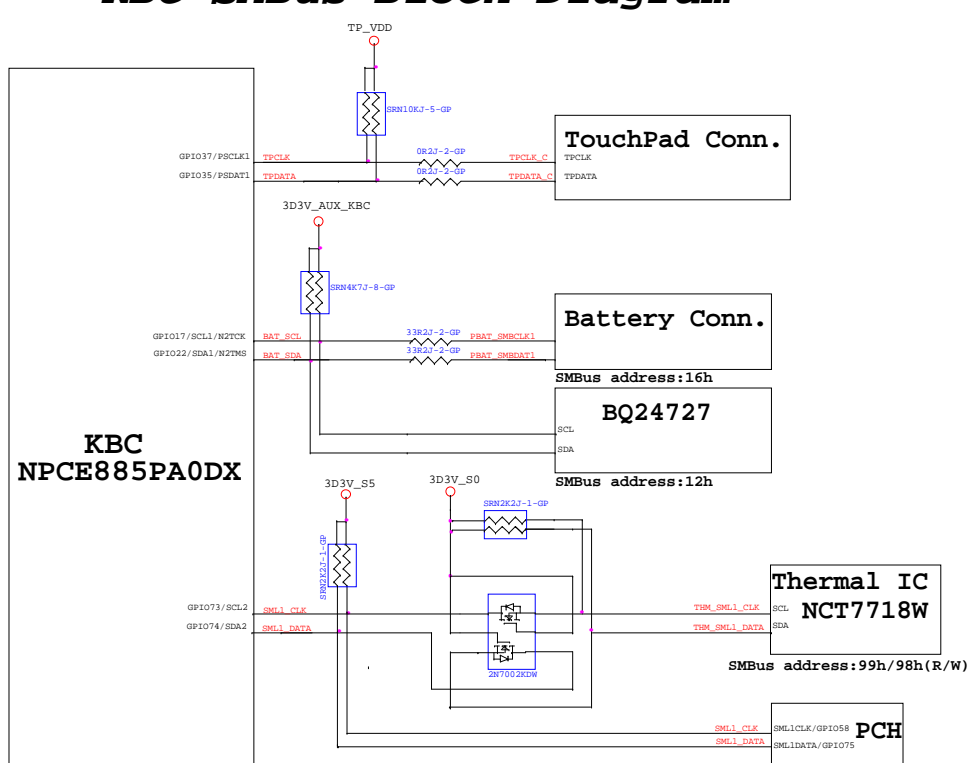
Title: **Power Block Diagram**

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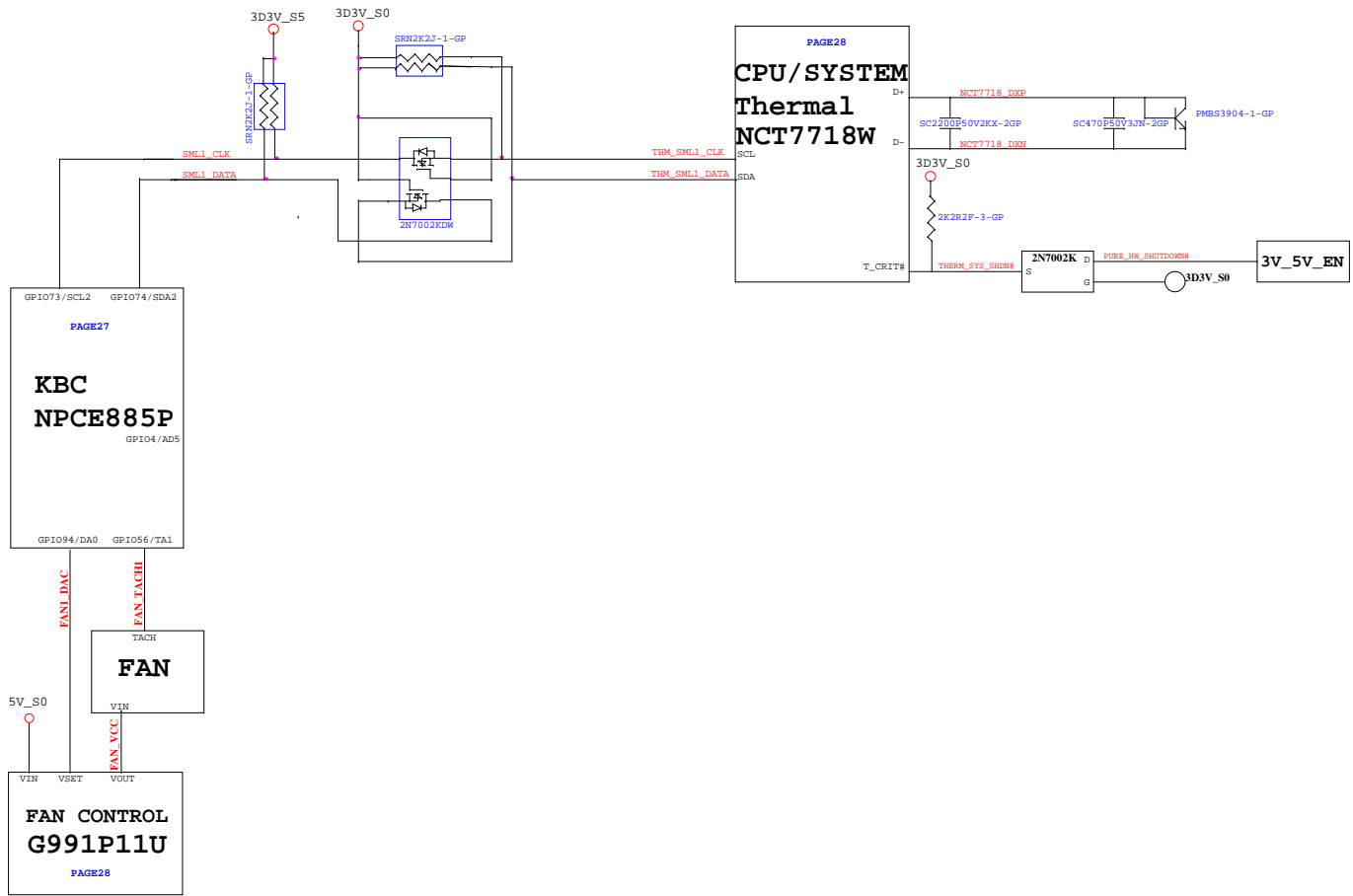
PCH SMBus Block Diagram



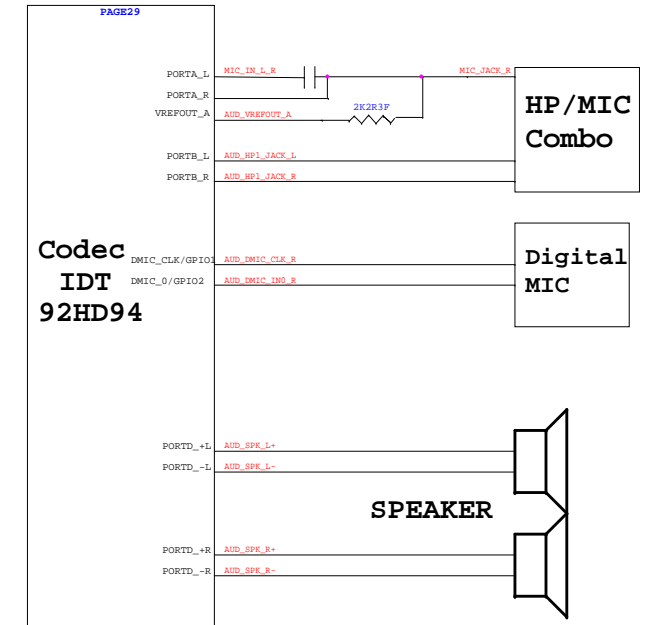
KBC SMBus Block Diagram



Thermal Block Diagram




Audio Block Diagram



DATE	PAGE	Change Item	Owner	Version
2011 11/28	92	Change VT358 AVDD power rail to 5V_S5 to avoid leakage	Power	X01
2011 11/28	92	Re-name Cap PC4663 to PC9218.	EE	X01
2011 11/28	85	Change U8506 power rail and select pin to 3D3V_VGA_S0 to avoid leakage	EE	X01
2011 11/28	93	Change PU9303 to 74.05930.03D by design	EE	X01
2011 11/28	93	POP PD9301, PD9302, PD9303, PD9304, PC9328, change PR9327 to 20K, PR9330 to 10K, PC9326 to 0.1u, PR9312 to 100K, PR9312 re-connect to DGPU_PWR_EN, PD9302 re-connect to DGPU_PWROK for GPU power sequence	EE	X01
2011 11/28	37	Change R3714 to 10K to fix step-like waveform	EE	X01
2011 11/28	84	DY R8408 cause GPU support PX5.0	EE	X01
2011 11/28	86	DY R8605, Q8602, R8603, R8604, U8601, U8602, U8603, U8604, cause GPU support PX5.0	EE	X01
2011 12/02	27	Reserved DGPU_PWROK signal to inform KBC	EE	X01
2011 12/02	62	POP R6208, DY R6201 for USB charging function.	EE	X01
2011 12/02	85	Change VRAM type setting.	EE	X01
2011 12/02	41	Change PT4101, PT4103, PT4104 to 77.52271.09L for design change	EE	X01
2011 12/02	27	Add R2737 for avoiding KBC power drop.	EE	X01
2011 12/02	37	Change R3719 to Q402 type	EE	X01
2011 12/02	69	Change TPAD1 conn by ME	ME	X01
2011 12/02	82	Change LEDBD1 conn by ME	ME	X01
2011 12/02	56	Change HDD1 conn by ME	ME	X01
2011 12/02	68	Change PWSW1 conn by ME	ME	X01
2011 12/02	27	Change RSTSW1 conn by ME	ME	X01
2011 12/02	39	Add BATSW1 and R3901 for avoiding MB crack on assembling.	ME	X01
2011 12/02	60	Change RTC1 conn by ME	ME	X01
2011 12/02	39	DY D3901, D3902, D3903 cause the battery is internal type.	EE	X01
2011 12/02	51	Re-name D5001 and F5001 to D5101 and F5101, and DY F5101 and add R5109 due to no current leakage problem	EE	X01
2011 12/02	14	Change DM1 conn by ME	ME	X01
2011 12/02	27	Change R2724 to 20K for X01 version	EE	X01
2011 12/02	85	DY C8523, cause VGA temp detect by SMBUS.	EE	X01
2011 12/02	28	DY U2803, C2817, C2818 cause VGA temp detect by SMBUS.	EE	X01
2011 12/02	38	Del PR3812.	EE	X01
2011 12/02	49	Change LCD1 conn by ME	ME	X01
2011 12/02	60	POP U6001 and del ROMSK1 for X01 version	EE	X01
2011 12/02	65	Change R6507 to J type	EE	X01
2011 12/02	39	Change BATT1 conn by ME	ME	X01
2011 12/02	82	Change IOBD1 conn by ME	ME	X01
2011 12/02	68	Add WLAN/WWAN LED power control circuit	EE	X01

DATE	PAGE	Change Item	Owner	Version
2011 12/09	27	Change AOAC_PCIE_WAKE# pull high to 3D3V_WLAN_AOAC and PCIE_WAKE# to 3D3V_LAN_S5	EE	X01
2011 12/09	66	Change WWAN power to 3D3V_S0	EE	X01
2011 12/09	8	Change VCC_CORE MLCC by power team request	Power	X01
2011 12/09	9	Change AXG_CORE MLCC by power team request	Power	X01
2011 12/09	22	Reserved DGPU_HOLD_RST# & DGPU_PWR_EN# pull high and down	EE	X01
2011 12/09	97	Follow EMI request added Cap.	EMI	X01
2011 12/09	20	Rename PCIE request pin	EE	X01
2011 12/09	65	Add WLAN requirist circuit	EE	X01
2011 12/12	40	design change PU4001 by Power team request	Power	X01
2011 12/12	41	design change PU4106 by Power team request	Power	X01
2011 12/12	41	Change PU4102 to colay symbol by Power team request	Power	X01
2011 12/12	45	Change PU4501to VT386 by Power team request	Power	X01
2011 12/12	46	Change PR4609 and PR4612 by Power team request	Power	X01
2011 12/12	48	Change PU4801 by Power team request	Power	X01
2011 12/12	43	Reserved PT4301 by Power team request	Power	X01
2011 12/12	84	Change R8412 to 4.7k.	EE	X01
2011 12/12	27	Change U2701 to new P/N	EE	X01
2011 12/13	82	Add ER8201, ER8202, ER8203, ER8204 by EMI request.	EMI	X01
2011 12/13	18	Reserved USB_PN13, USB_PP13 test point.	EE	X01
2011 12/13	62	Del USB3.0 Redriver circuit.	EE	X01
2011 12/13	27	Change R2735 and R2737 to 20K for fix AUX power overshoot.	EE	X01
2011 12/13	41	Change PC4127 to 4.7uF for fix AUX power overshoot.	EE	X01
2011 12/13	82	Add ER8205, EC8206 by EMI request.	EMI	X01
2011 12/13	46	Add EL4601, EL4602 by EMI request.	EMI	X01
2011 12/13	43	Add EG4301,EG4302EG4303,EG4304,EG4305,EG4306,EG4307 by EMI request.	EMI	X01
2011 12/13	44	Add EG4401,EG4402,EG4403,EG4404,EG4405,EG4406,EG4407 by EMI request.	EMI	X01
2011 12/13	15	Change DM2 conn by ME request	ME	X01
2011 12/15	97	Add EC9736, EC9726, EC9750 EC9708, EC9709, EC9770, EC9705, EC9769 by RF request.	RF	X01
2011 12/15	56	Add EC5601 by RF request.	RF	X01
2011 12/15	46	Add EC4638 by RF request.	RF	X01
2011 12/15	31	Add EC3122 by RF request.	RF	X01

<Core Design>



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DATE	PAGE	Change Item	Owner	Version
2011 12/15	14	Change DM1 P/N to 62.10017.S81	EE	X01
2011 12/15	15	Change DM2 P/N to 62.10017.T01	EE	X01
2011 12/15	62	Del R6201 change by USB detect function	EE	X01
2011 12/15	65	DY R6507, U6501 for design change	EE	X01
2011 12/15	68	Add R6809, DY C6802, R6803, D6802, WLAN LED power control by AOAC_WLAN_EN#.	EE	X01
2011 12/15	8	Change C825, C830, C831, C832 to 0805 type.	EE	X01
2011 12/15	9	Change C906, C907, C908, C909, C910 to 0805 type.	EE	X01
2011 12/15	93	Del 1D8V_VGA_S0 power good circuit.	EE	X01
2011 12/15	83	Del VGA_RST# circuit.	EE	X01
2011 12/15	86	Del 1D5V_VGA_S0 power good circuit.	EE	X01
2011 12/15	31	Reserved EC3101 by RF request.	RF	X01
2011 12/15	97	Reserved EC9771, EC9772 by RF request.	RF	X01
2011 12/16	86	Change C8642, C8650, C8647 to 22u 0805 size.	EE	X01
2011 12/16	62	Pop TR6204, DY R6279, R6280.	EMI	X01
2011 12/16	49	Pop TR4902, DY R4903, R4906.	EMI	X01
2011 12/16	8	Change C847 to 22u 0805 size.	EE	X01
2011 12/16	68	Pop C6802, for soft start.	EE	X01
2011 12/19	38	Change PC3806 to 0805 type	Power	X01
2011 12/19	43	Del PT4301 cause no layout area.	Power	X01
2011 12/20	44	Change PWR_GFX to PWR_CPU	Power	X01
2011 12/20	18	Change touch panel USB signal to port 4.	EE	X01
2011 12/20	82	Reserved TPAN1, and swap IOBD1's main and 2nd source.	EE	X01
2011 12/20	49	Swap LCD1's main and 2nd source.	EE	X01
2011 12/20	14	Change R1401, R1402 to short pad	EE	X01
2011 12/20	15	Change R1502 to short pad	EE	X01
2011 12/20	39	Change R3902, R3903, R3904 to 100 ohm to avoid break KBC when battery in.	EE	X01
2011 12/20	27	Del RN2703, add R2714, R2715.	EE	X01
2011 12/21	48	POP PR4814, change PR4811 to 365ohm, PR4813 to 100Kohm	Power	X01
2011 12/21	21	Add R2115 and del R6001 for SPI louting setting	EE	X01
2011 12/21	8	DY C807, C843, C824.	Power	X01
2011 12/21	42	Change PR4236 to 374ohm, PR4249 to 7.68Kohm.	Power	X01
2011 12/21	43	Change PU4301 IC to lastly version.	Power	X01
2011 12/21	44	Change PU4401 IC to lastly version.	Power	X01
2011 12/21	40	Design change PU4002 by power request	Power	X01
2011 12/21	27	Add R2716 to modify PSL circuit.	EE	X01
2011 12/23	82	Swap USB1, USB10 signal to TR8202 TR8201 for layout	EE	X01

DATE	PAGE	Change Item	Owner	Version
2011 12/23	62	Swap USB0 signal to TR6204 for layout	EE	X01
2011 12/23	97	Del H8.	ME	X01
2011 12/27	51	Pop D5101, DY R5109.	EE	X01
2011 12/30	93	Change PD9301, PD9302, PD9303, PD9304's 2nd source to 83.R5003.H8H	EE	X01
2011 12/30	31	Change U3101 to 71.08162.A03 due to vendor update new version.	EE	X01
2011 12/30	97	Pop EC9738, EC9739, EC9741, EC9743, EC9744, EC9764, EC9765, EC9766, EC9767, EC9768	EMI	X01
2011 12/30	36, 93	Change U3601 U3602 PU9305 PU9306 2nd to 84.04178.037	Power	X01
2011 12/30	49	Change TR4902 to 69.10103.041	EMI	X01
2012 01/09	15, 24	DY C1507 and C2403 by PI testing result.	EE	X01
2012 01/09	48	Change VCCSA to LDO type.	Power	X02
2012 01/09	51	Change HDMI SMBUS pull up power to 5V_HDMI_S0_R	EE	X03
2012 01/30	48	Reserved PC4818 PC4819 to prevent VCCSA power IC VID setting(PWM solution)	EE	X03
2012 01/30	68	Add D6803 to fix DW1703 BT LED behavior. and change WLAN LED power rail to 5V_S0.	EE	X03
2012 01/30	97, 38	Take off EC9704, del PS_ID_R.	EE	X03
2012 01/30	82	Move IO BD conn signal for coaxial cable	EE	X03
2012 01/30	66	DY R6615.	EE	X03
2012 01/30	40, 38	Change PR4004 to 3K and PR3816 to 3.3K for hiccup mode adaptor.	EE	X03
2012 01/30	62	Change U6201 to lastly version.	EE	X03
2012 01/30	31	Change L3101 to prevent the shortage problem.	EE	X03
2012 02/06	82	Change TPAN1 P/N by ME request and modify conn pin define.	EE	X03
2012 02/06	31	Reserved C3110 for Lan IC.	EE	X03
2012 02/06	5, 8, 9, 14, 15, 19, 23, 24, 27, 28, 36, 37, 38, 49, 51, 62, 65, 66, 83, 85	Change R504, R812, R909, R1404, R1405, R1505, R1503, R1921, R1916, R1924, R1929, R1925, R2304, R2301, R2307, R2306, R2308, R2403, R2404, R2412, R2402, R2702, R2765, R2794, R2778, R2792, R2733, R2767, R2768, R2720, R2764, R2723, R2727, R2807, R3614, R3710, PR3819, R4912, R4913, R5125, R5101,R5102, R5149, R5103, R5108, R5107, R5106, R5105, R6202, R6203, R6204, R6205, R6505, R6502, R6616, R8322, R8504, R8506, R8507, to short pad	EE	X03
2012 02/10	41, 42, 45, 46, 47, 95	Change PR4127, PR4130, PR4133, PR4116, PR4251, PR4250, PR4212, PR4207, PR4228, PR4523, PR4522, PR4510, PR4511, PR4626, PR4621, PR4622, PR4623, PR4611, PR4602, PR4702 ,PR9215 to short pad	Power	X03
2012 02/13	51	Change HDMI output power design	EE	X03
2012 02/13	41, 42, 18 19, 28, 93	Change PR9311, PR9320, PR4116, PR4219, PR4223, PR4252, PR4254, PR4261, R1823, R1927 R2813 to short pad	Power	X03
2012 02/13	97	Add EC9704, EC9706, EC9716, EC9718, EC9722, EC9724, EC9728, EC9730, EC9775, EC9776, EC9773, EC9774,EC9701, EC9751, EL4901 by EMI required	EMI	X03



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